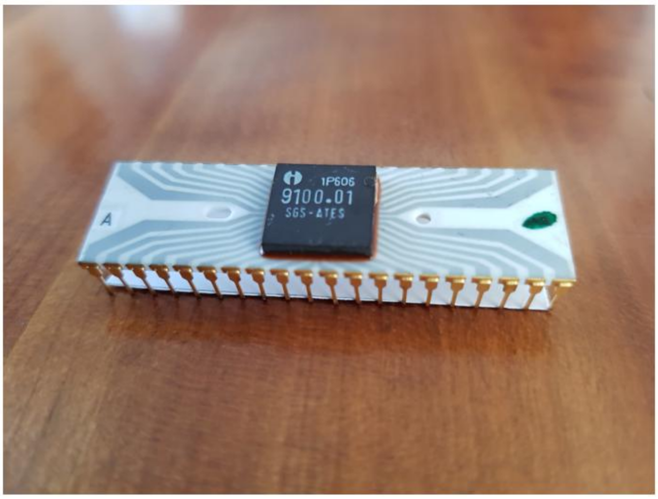
CP3-F



Around 1970, the Olympia Werke in Braunschweig introduced the self-developed 8-bit microprocessor CP3-F, which made it possible to create computers with only two components – a level of complexity that was unique at the time.

Historical / technological background

Olympia Werke (a subsidiary of AEG) was one of the largest manufacturers of office equipment. The main plant in Wilhelmshaven produced mechanical and electromechanical typewriters, while the Braunschweig plant developed and manufactured display and printing calculators for primarily commercial applications. Thus, the Braunschweig plant focused on the development of electronic circuits.

Around 1960, a display calculator like the "RAE4" from Olympia had a mass of 13 kg. The electronics, constructed with discrete components, were housed in a desk-shaped case measuring 38 cm wide, 42.5 cm deep, and 21 cm high—a true heavyweight. If you imagine a desk with a typewriter and such a computer on it, there would be hardly any work space left. Thus, there was an urgent need to develop more compact computers. Replacing the discrete components with TTL ICs brought some improvements, but it was still not a breakthrough.

Higher integration was made possible by ICs that were implemented with MOS transistors instead of bipolar ones. Olympia developed a computer chip called the "CP1-F," which allowed for the construction of significantly smaller computers. The "CP" part of the name, incidentally, stands for Calculator Printer, thus reflecting the direction of the development.

A disadvantage of this computer IC was that it was difficult to cover a wide range of computer variants. New functionalities would have required the development of a new component – a significant effort. With earlier computers, only one or more boards would have had to be changed, which would have been possible relatively quickly. The rest could have been reused. Thus, the space savings came at the cost of a loss of flexibility.

This is how the idea for the development of the CP3-F microprocessor came about. A modular concept was developed in which a central processing unit (RSE) with the functions of CPU, RAM, and I/O ports could be used unchanged for all future devices. The device-specific programs were stored in a second "ROM"
The program was stored in a "PSE" (Program Storage Unit) chip, which contained a mask-programmed 1KB ROM and two I/O channels. The chip was designed so that only the topmost metallization layer contained the program content, while the remaining layers remained unchanged. This reduced the effort required to create new

Program versions are few and the time between program creation and delivery of the first components is short.

For applications with greater program or data memory requirements, the system was supplemented by two additional modules: a “DSE” (Data Storage Unit) with 128 bytes of RAM and one 8-bit I/O channel, and a ROM/RAM module with 768 bytes of ROM, 18 bytes of RAM, and two 8-bit I/O channels.

For comparison: At about the same time as the CP3-F processor, Intel released the 8008 (according to Wikipedia, "Intel 8008 on April 1, 1972"). Like the CP3-F, the 8008 was also built using PMOS technology; both had a system clock speed of 800 kHz and an address range of up to 16 KB. However, the 8008 was a pure CPU; it had no RAM (apart from a few registers) and no I/O ports. Addresses and data were transferred sequentially over an 8-bit bus and had to be separated externally using control signals. This meant that more components were required for a minimal configuration—a significant disadvantage.

Up to 15 modules could be connected to the CP3-F's PSE, allowing even larger systems to be implemented. One example was a typewriter in which the keyboard was made up of individual switches arranged in a matrix and then queried and evaluated by the processor. The necessary debouncing was also performed via software. Stepper motors, controlled directly by the program, drove the head carriage and the paper feed. There were only power output stages, but no other controller modules. The magnets for the ball head movement and the downstroke were also controlled by the program. Even the 1 kHz tone, which replaced the usual bell when the edge of the area was reached, was generated by program loops. The system's reserves were even sufficient to drive an external tape storage device for storing document templates and text modules, for applications as a text machine.

Provider of the CP3-F

The CP3-F processor was produced by three companies. In addition to the AEG subsidiary Telefunken, the CP3-F was manufactured by SGS ATES (now STM) and General Instruments (now Microchip). Each manufacturer developed its own chip design to suit its production lines, which is why the chip sizes of all three manufacturers differ significantly. Nevertheless, the components were fully interchangeable, and mixed components from different manufacturers could easily be used in devices.

Although the CP3-F was developed by Olympia for its own use in Olympia products, after an introductory period, all manufacturers were free to offer the CP3-F on the market. SGS ATES introduced it to a broad audience at Seminex 1975 under the designation M38. General Instruments listed the components in data books under the designation LP8000.

The modular system concept

For such a sophisticated system concept, it is important to know which functions are contained in which components. For reasons of manageability, a package size of 40 pins was chosen. Five of the pins are required for clock, reset, and the two supply voltages typical for PMOS components. The 8-bit wide data bus should not be multiplexed with other signals. At least one 8-bit wide I/O channel should also be provided.

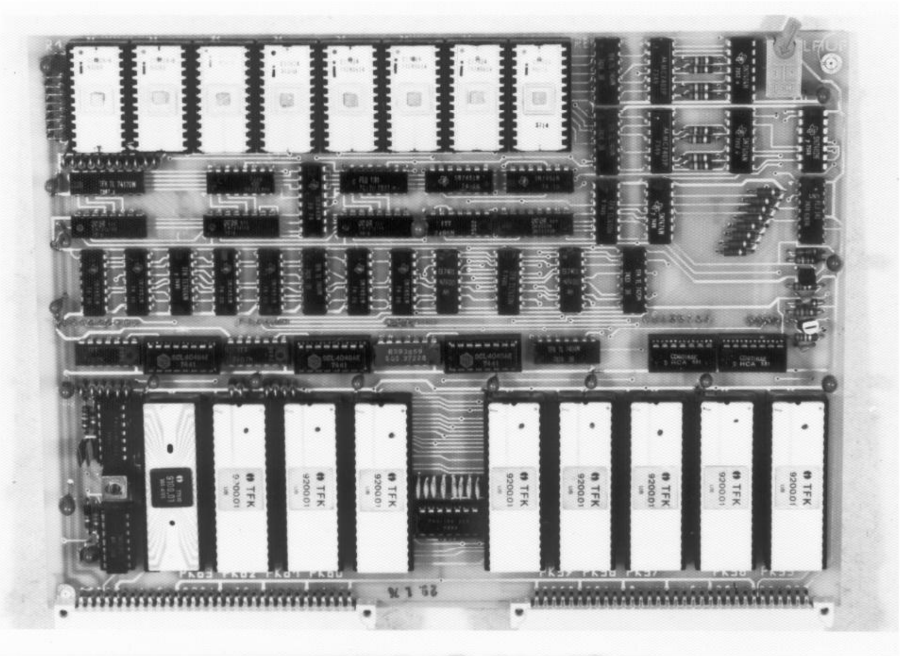
should be available. To ensure that as many pins as possible are available for I/O channels on the other system components, the address counters were moved to the peripheral compone
Only when these need to be loaded during jumps is the transfer via the data bus. Four control signals are used to synchronize the address counters and control access. In order to distribute the 16 KB address space among components with different memory capacities, the address range is divided into 64 segments of 256 bytes each, which are addressed by the RSE via six address lines. This sounds more complicated than it actually is. A PSE with 1 KB ROM detects whether it is currently being "addressed" by the upper four of the six address lines. The lower two lines, together with the internal address registers, are used for internal addressing.

A description of the CP3-F was published in the "Elektronik" special issue "Mikroprozessoren" (Microprocessors) in 1977 on page 48 under the title "The First European Microprocessor." The author of the article, Jürgen Sorgenfrei, oversaw the development of the CP3-F as head of design.

Development aid for the CP3-F

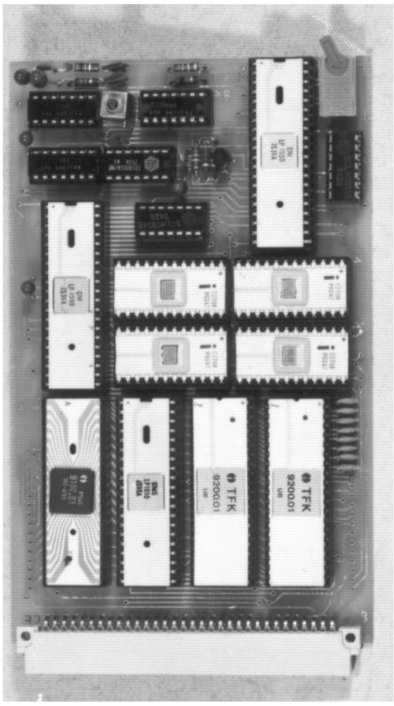
A development environment is essential for professional software creation. Olympia used a macro assembler written in Fortran IV as its development environment, running on an IBM 370 mainframe. The programs were also tested using a simulation program that implemented each machine instruction and calculated the respective register contents of the accumulator, status register, address counter, RAM, and I/O ports. Keyboard input and output to the display and printer were simulated using graphics computers connected to the mainframe. While these tools allowed the program logic to be verified, they could not verify real-time behavior.

To test the entire system behavior, the system components had to be simulated in hardware. The first electrically programmable PROMs were just becoming available on the market. Thus, the address registers and status decoding of the system components were simulated using TTL components. On a double Eurocard, eight 256 x 8-bit PROMs (Intel 1702) served as program memory and were connected via this logic to the data bus of the RSE, which was also housed on the card. Eight DSE components served as I/O ports and, if necessary, as RAM expansion. This allowed software to be tested in real time, and the simulation behaved exactly like the later components.



Prototype construction with replica of the address counters using TTL components

General Instrument also recognized the need for a good test environment and created its own LP1010 memory interface specifically designed for the system. This module was essentially a modification of the PSE. The only difference is that the ROM was removed and the addresses were routed out, allowing them to be used for external memory modules. Each of these LP1010 modules could supply a memory area of 2 KB. Using two of these modules, an RSE, two DSE modules, and four 2708 PROMs (each with 1 KB), a Eurocard-sized module was constructed, allowing most applications to be tested. The data bus on this module was routed to adapter connectors, allowing additional modules to be connected if more program memory, more I/O channels, or more RAM was needed. These modules also made it possible to create configurations without creating mask-programmed program memory modules. This meant that the CP3-F could also be used for standalone applications.



Prototype map in European format

As an office machine manufacturer, Olympia had little inclination to market the system to end customers and provide the necessary support. The small company System Elektronik recognized the potential and developed its own card – also in Eurocard format – containing an RSE, a memory interface module, two I/O modules, and eight 1702 PROMs, each with 256 bytes of program memory. This card, too, was expandable via adapter plugs. The company also developed an assembly program that ran on this card (with an attached RAM memory expansion), thus eliminating the need for assembly on a mainframe. They also supported customers with training courses on programming in the assembly language of the CP3-F and built systems for customers that used this processor as a control unit.

The F8 microprocessor as the “successor” to the CP3-F

Interrupt and timer structures had already been planned during the development of the CP3-F, but these were initially unfeasible due to the space requirements. It was soon recognized that a transition from PMOS to NMOS seemed sensible due to the smaller space requirements of the structures. As early as 1975, a RAM memory module, the "DSE2," was designed, which had four times the memory capacity.

The CP3-F system was naturally followed closely in specialist circles, and so it is not surprising that Fairchild's F8 microprocessor came onto the market, a microprocessor that bore a striking resemblance to the CP3-F in many respects. The "3850" CPU also had 64 bytes of RAM (the CP3-F only had 48 bytes), and two I/O ports were also available, one more than the CP3-F. As with the CP3-F, there was also a "3851" program memory unit, which contained the program ROM, the address counter, and two I/O channels. A "3853" memory interface also enabled the connection of standard memory modules. For use as a microcomputer in Eurocard format, there were also "3861" PIO modules, which contained two I/O ports. In addition to the CPU, the other modules each housed an interrupt input and a timer.

Based on the F8, MOSTEK announced the "Single Chip Microcomputer MK3870" in July 1977, essentially a CPU and a program memory unit on a single chip. The 3870 had 64 bytes of RAM, 2 KB of program memory, four 8-bit I/O ports, a timer, and an external interrupt. The instruction set was fully compatible with the F8. A version was available for development purposes in which a PROM could be plugged onto the top of the case. The 3870 was used in numerous keyboards, heating controls, printers, and control panels for televisions and hi-fi equipment.