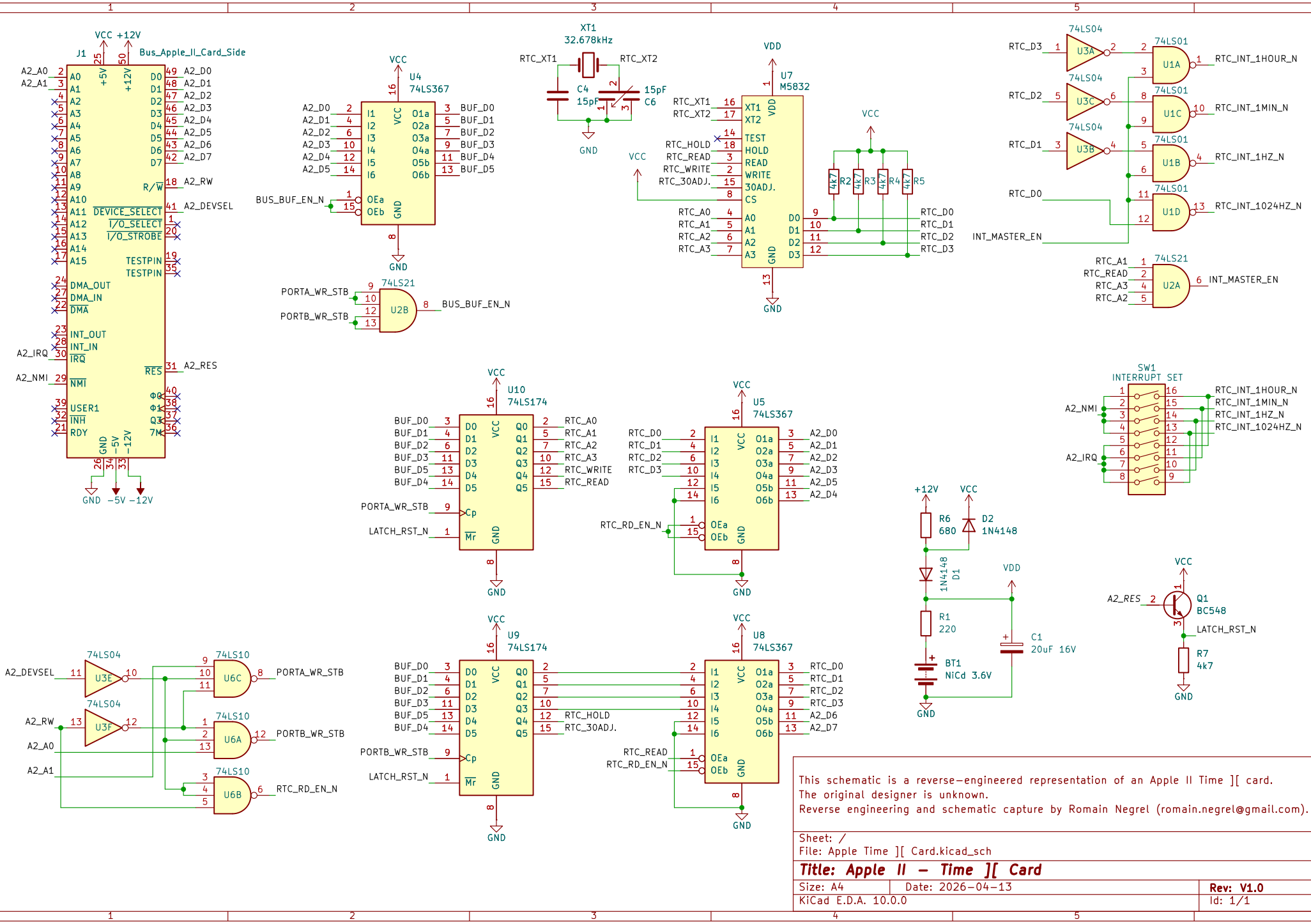
J1
Bus_Apple_II_Card_Side
VCC +12V
GND −5V −12V
A2_A0
A2_A1
A2_IRQ
A2_NMI
A2_RW
A2_RES
A2_DEVSEL
A2_D0
A2_D1
A2_D2
A2_D3
A2_D4
A2_D5
A2_D6
A2_D7
R/W
DEVICE_SELECT
I/O_SELECT
I/O_STROBE
TESTPIN
DMA_OUT
DMA_IN
DMA
INT_OUT
INT_IN
IRQ
NMI
USER1
INH
RDY
U4
74LS367
BUS_BUF_EN_N
BUF_D0
BUF_D1
BUF_D2
BUF_D3
BUF_D4
BUF_D5
U2B
74LS21
PORTA_WR_STB
PORTB_WR_STB
XT1
32.678kHz
RTC_XT1
RTC_XT2
C4
15pF
C6
U7
M5832
RTC_HOLD
RTC_READ
RTC_WRITE
RTC_30ADJ.
RTC_A0
RTC_A1
RTC_A2
RTC_A3
RTC_D0
RTC_D1
RTC_D2
RTC_D3
R2
R3
R4
R5
4k7
U3A
U3B
U3C
U1A
U1B
U1C
U1D
74LS04
74LS01
RTC_INT_1HOUR_N
RTC_INT_1MIN_N
RTC_INT_1HZ_N
RTC_INT_1024HZ_N
INT_MASTER_EN
U2A
74LS21
U10
74LS174
LATCH_RST_N
U5
74LS367
RTC_RD_EN_N
SW1
INTERRUPT SET
R6
680
D2
1N4148
D1
R1
220
BT1
NiCd 3.6V
C1
20uF 16V
Q1
BC548
R7
4k7
U3E
U3F
U6A
U6B
U6C
74LS10
U9
U8
This schematic is a reverse-engineered representation of an Apple II Time][card.
The original designer is unknown.
Reverse engineering and schematic capture by Romain Negrel (romain.negrel@gmail.com).
Sheet: /
File: Apple Time][Card.kicad_sch
Title: Apple II – Time][Card
Size: A4
Date: 2026-04-13
KiCad E.D.A. 10.0.0
Rev: V1.0
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