Chapter 1
Introduction

ICKY is a multiple resolution video card for the Macintosh II PDS computers. Supported monitors include the Macintosh 13 inch, the Macintosh 12 inch, and the Bartlett internal SE/30 gray scale adapter. The card supports 1, 2, 4, 8, and 24 bit mode. Virtual video modes are supported, which allows large virtual screens to be displayed via hardware pan. The Maverick chip is used to do all PDS, VRAM, and Video timing.

Chapter 2
Macintosh II PDS Family

The Macintosh SE/30 contains the Motorola 68030 microprocessor and one expansion slot, which may be numbered 9, A, or B hex. The SE/30 is essentially a Macintosh IIx computer in a smaller box. The expansion slot, though, comes off of the processor bus. The SE/30 does not have any NuBus expansion slots.

While the Macintosh SE/30 has 32 address lines, only 24 of these are used in the normal (default) mode. The computer can be placed in 24-bit or 32-bit mode similar to the Macintosh II. The 8-bit video board's ROM and VRAM array addresses, however, are all directly accessible in normal mode.

Address	Description
00000000 - 000FFFFF	RAM (minimum configuration)
00100000 - 00CFFFFF	RAM (expansion area)
00D00000 - 3FFFFFFF	RAM (undefined)
40000000 - 4007FFFF	ROM Bank 0 (minimum configuration)
40080000 - 4FFFFFFF	ROM (undefined)
50000000 - 50001FFF	VIA1 (x0200)
50002000 - 50003FFF	VIA2 (x0200)
50004000 - 50005FFF	SCC (x0002)
50006000 - 50007FFF	SCSI (Handshake)
50010000 - 50011FFF	SCSI (x0010)
50012000 - 50013FFF	SCSI (Pseudo DMA)
50014000 - 50015FFF	Sound
50016000 - 50017FFF	SWIM
50018000 - 57FFFFFF	(undefined)
58000000 - 5FFFFFFF	030 Direct Slot expansion (if pseudo-NuBus is not used)
60000000 - F8FFFFFF	expansion (undefined)
F9000000 - FBFFFFFF	expansion pseudo-NuBus slots
FC000000 - FDFFFFFF	expansion (undefined)
FE000000 - FE00FFFF	video RAM space
FEFF0000 - FEFFFFFF	video ROM space
FF000000 - FFFFFFFF	expansion (undefined)

Table 2-1 Address Mapping

The Macintosh SE/30 uses memory-mapped I/O. Each device in the system can be accessed by reading or writing to specific address locations in the address space of the computer. The addressing for a card in a slot is directly dependent on the slot number. The SE/30 has three slot numbers possible for a single slot. The slot number is defined in hardware on the expansion board and cannot be changed.

The slot in the Macintosh SE/30 can be directly accessed in the 32-bit mode at the address found by multiplying the slot ID by 10,000,000 hex (s000 0000-sFFF FFFF hex); this is the Super Slot Space. The slot can also be found at the Slot Space Fs00 0000-FsFF FFFF hex (s = slot ID, 9-B) when in the 24-bit default operating mode. Each physical slot has both the slot and super slot space allocated to it. In 24-bit mode the AMU (Address Mapping Unit) or PMMU (Paged Memory Management Unit), whichever is present, will convert s0 0000 to Fs00 0000.

2.1 Bus Signals

The Macintosh SE/30 Direct Slot expansion bus is based on the Motorola 68030 microprocessor. It is machine-specific, not a general-purpose bus like NuBus. The card design may be similar to NuBus (Pseudo-NuBus), with the same type of ROM and addressing, but the pinout and signals differ. The SE/30 Direct Slot uses a 120-pin 16MHz synchronous bus. Words, halfwords, and bytes can be read and written, but the bus is optimized for word transfers. All signals are active low.

Bit 31			Bit 0
Direct Slot Word			
Halfword 1		Halfword 0	
Byte 3	Byte 2	Byte 1	Byte 0

Table 2-2 Bus Data

The bus specification divides the signals into five types:

Power: +5V, +12V, -12V, and -5V.
Data and Address Lines: A0-A31, D0-D31.
Control Lines: \STERM, SIZ0-SIZ1, FC0-FC2, \RESET, \BERR, R/W, \AS
Clocks: CPUclock and C16M (for the SE/30, these are identical 16 MHz signals).
Machine-Specific Signals: PWROFF, \BUSLOCK, \IRQ1-\IRQ3, \TM0A-\TM1A, \NuBus, CPUclock.

The connector contains three rows of pins (see Appendix B). The Micron video board does not use all of the signals on the expansion bus. A 'high' level is > 2V, 'low' level < 0.8V.

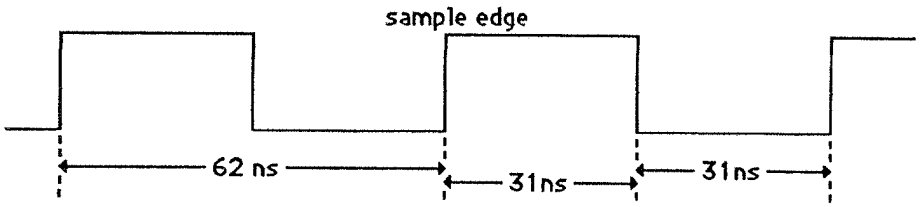


Figure 2-1 System Clock

2.2 READ-WRITE-READ CYCLE

The read-write-read transaction is shown below. It may take longer than shown, but the timer on the SE/30 main logic board will generate a bus error signal when the address strobe is asserted for longer than ≈20 microseconds.

SE/30 Read/Write Cycles
(All accesses to the video card are 32 Bit Synchronous)

Read Cycle

At state zero (S0) the SE/30 drives Ax, FCx, SIZx, and R\W with an address, type of function, size of data transfer, and read command. Half a clock cycle later, during state one (S1), \AS and \DS are asserted by the SE/30 to tell the external device that the address lines are now valid and data may be placed on the bus. By the end of S1 the external device will assert \STERM. \STERM tells the SE/30 that the read data will be valid by the next falling clock. At the start of state two (s2) the external device places data on the bus and terminates \STERM. The SE/30 latches in the data at the end of S2. State three (S3) provides the data hold time as required.

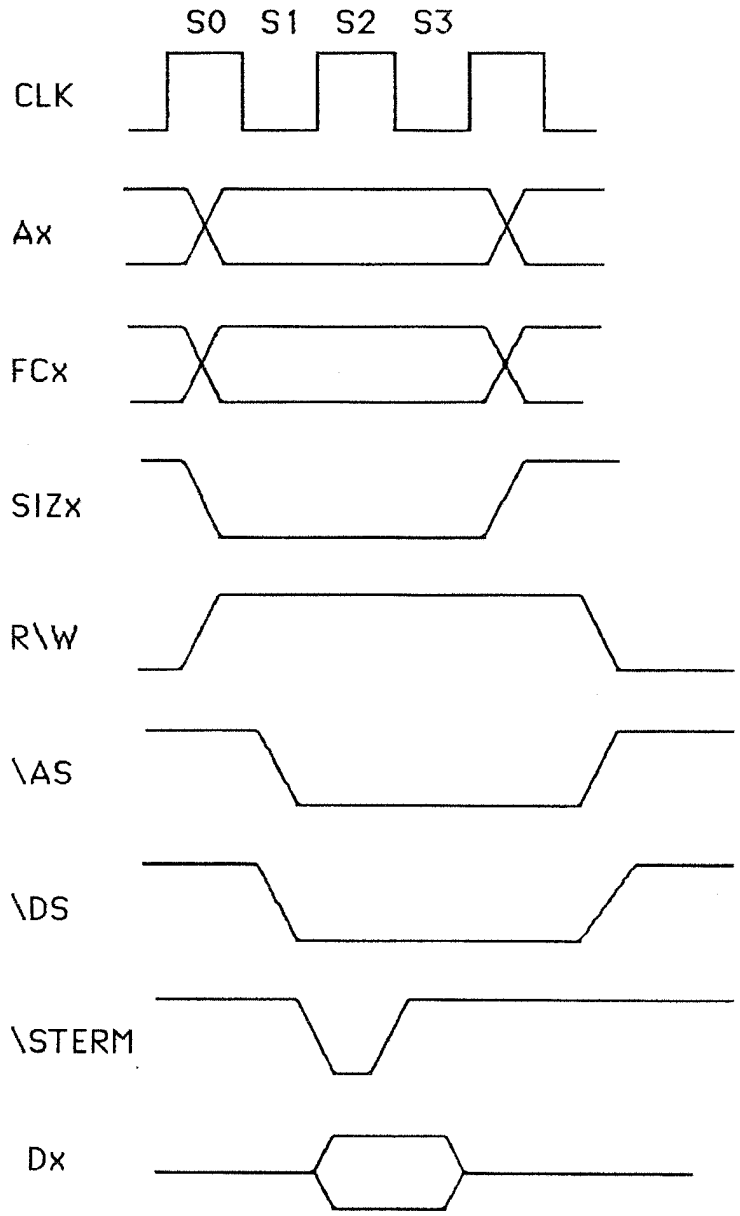


Figure 2-2 SE/30 32 Bit Synchronous Read

Write Cycle

At state zero (S0) the SE/30 drives Ax, FCx, SIZx, and R\W with an address, type of function, size of data transfer, and write command. Half a clock cycle later, during state one (S1), \AS is asserted by the SE/30 to tell the external device that the address lines are valid. At the beginning of state two (S2) the SE/30 looks for \STERM. If \STERM is not present the SE/30 will insert a wait state. Also during S2 the SE/30 will drive the data bus with valid data. During a wait state (SW) the SE/30 asserts \DS to tell the external device that the bus still contains valid data. At the start of each wait state the SE/30 will check for \STERM. If \STERM is not present the SE/30 will insert another wait state, if

\STERM is present, the SE/30 will terminate the write cycle in the following state (S3). During state three (S3) the address and data lines remain valid.

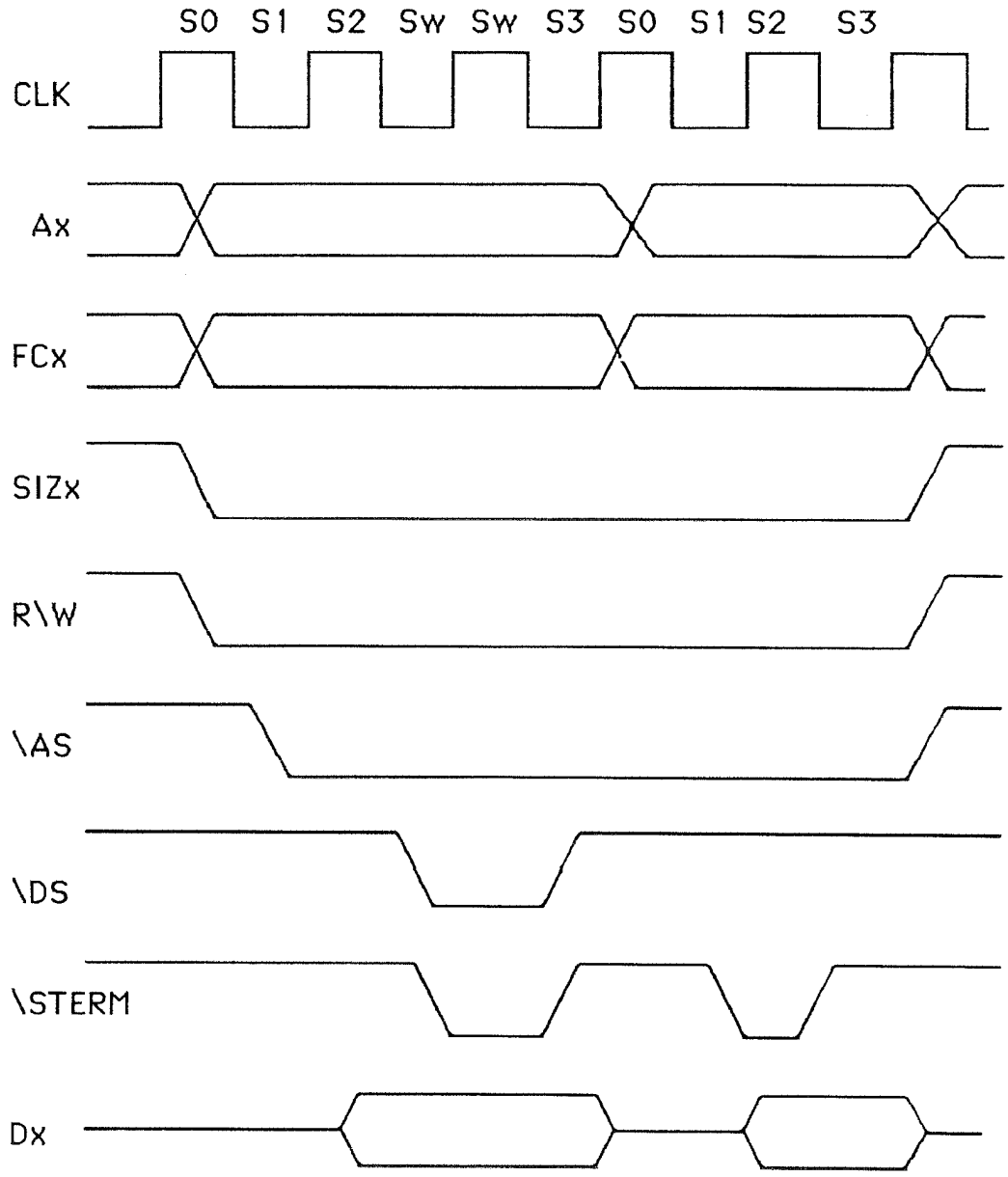


Figure 2-3 Read-Write-Read Cycles

2.3 System Board

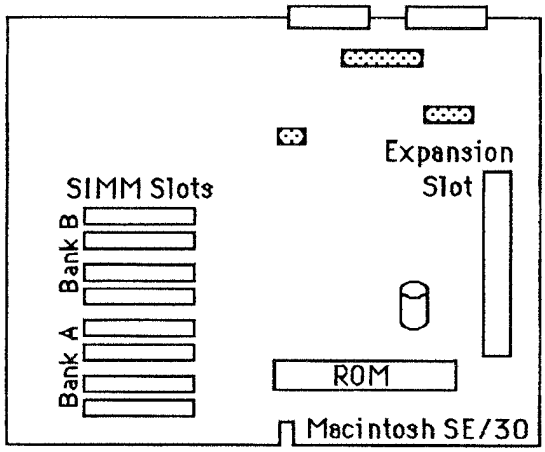


Figure 2-4 Macintosh SE/30 System Board

Chapter 3
Theory of Operation

3.1 PDS Interface

3.2 Video Ram Control

3.3 Pixal Data Formatting

3.4 RGB Video Output

3.1 PDS Interface

The BIVT controls the operation of the PDS interface. Four 74F245s are used to buffer the data and three 74ALS373s are used to latch the address.

For VRAM access the BIVT will generate all timing for RAS, CAS, row and column muxing. Only one RAS is used on Icky. Two CASs are used to support the 2 way interleaved memory. The BIVT will hold off access to the VRAM if a VRAM transfer cycle is needed.

For ROM reads the BIVT will generate the ROMCS signal.

For DAC access, the BIVT will generate DACRD and DACWT signals. DAC access will be held off during active video if the NOSNOW bit is enabled within the BIVT.

Also the BIVT will accept writes to its internal registers. These are used to control the operation and configuration of the BIVT.

3.2 Video Ram Control

All video ram control except SC0 and SC1 is provides by the BIVT. For bus access, the row and column address are muxed in three external 74F257s. For transfer cycles the BIVT generates the row and column addresses. Refresh is also generated by the BIVT.

3.3 Pixel Data Formatting

The VRAM is organized as two 32 bit wide interleaved banks. The two banks are capable of providing 4096 bytes per row. The pixel data is clocked out of the VRAMS by two out of phase clocks SC0 and SC1. The data then enters a 64 to 32 bit mux comprised of 8 74F257s. The mux alternates between the two banks and is controlled by PDBSEL. After the mux, the data can take one of two paths depending on if it is in 24 or 8 bit mode. Also note 1, 2, and 4 bit modes are just processed 8 bit mode. The first path is for 24 bit mode. Here the data bits 8 through 23 pass directly to the DAC. Bits 24 through 31 are ignored and bits 0 through 7 are passed through a mux and on to the DAC.

In 8 bit mode, the pixel data is routed through a 32 to 8 bit mux. The mux is comprised of 4 74F253s. PBSEL0 and PBSEL1 control which one of four bytes is selected. After the mux, the data is registered in a 74F374 to provide enough setup time for the pixel mixer pal. The pixel mixer pal will then format and shift the data out depending which mode is selected. The output of the pixel mixer is passed through a mux on to the DAC.

U25 generates all signals to control the muxes, shift clocks, and pixel mixer pal. FORRUN is the signal generated in the BIVT which signals when to start a new video line running.

3.4 DAC

The pixel data is converted to an analog voltage using a 473 DAC (U45). This DAC is capable of accepting either 24 bits of data for true color operation, or 8 bits for pseudo color. Also when in 8 bit mode, individual bits can be masked off, thus allowing support for 1, 2, and 4 bit modes. The selection of 8 or 24 bit mode is accomplished with the mode2 signal.

Along with the pixel data, sync and blank signals are also supplied to the DAC. These two signals are generated in the BIVT asic.

The BIVT generates the DAC read and DAC write signals which read and write the control registers inside the 473 DAC.

Figure 3-10 Video Generation Block Diagram

The following diagram illustrates the operation of a video D/A. In practice the blanking and sync intervals will be longer.

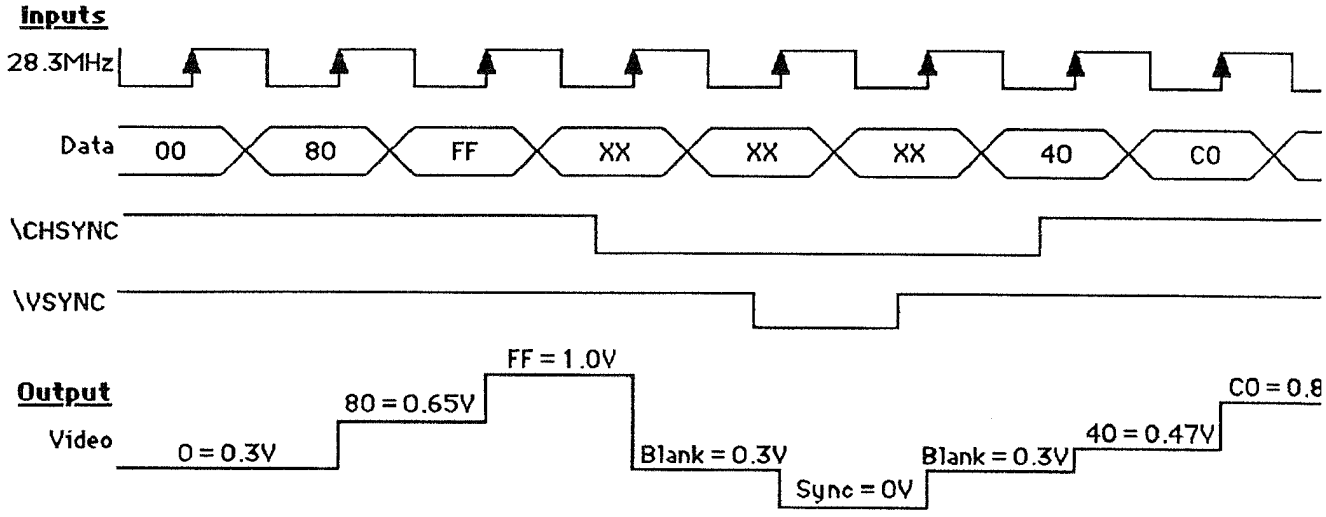


Figure 3-11 Video D/A Operation

More complete and detailed video diagrams can be found in the Electronic Industries Association specification EIA-343-A.

Appendix C
Maverick Theory of Operation

Introduction:
The Maverick gate array is designed for use on Macintosh video boards. It includes both SE/30 and NuBus bus interface circuits, and video timing generation circuits.

There are currently three different bond options for the chip. All inputs and outputs are available in the 'Top Gun' 120-pin option. NuBus-specific signals are not present on 'Goose' which is an SE/30 only 100-pin option. SE/30 specific interface signals are not present on 'Maverick' which is a 100-pin NuBus only option. It is expected that the 120-pin option will not be used in production unless problems are encountered in one or both of the 100-pin options (insufficient power and ground pins, noise, etc.). For the purposes of this document all versions of the chip will be referred to by the common name Maverick.

Bus Interface:
The bus interface includes address decoding for ROM, VRAM, DAC, internal mode registers and external mode registers.

ROM accesses are decoded for the top two megabytes of the slot address space. A ROMCS strobe of approximately 250 nanoseconds will be generated to enable the ROM data to the data bus unless a VRAM transfer cycle is being performed. If a VRAM transfer cycle is being performed the ROM cycle will be held off until the transfer is complete, and then the ROM cycle will occur.

DAC accesses are decoded for the next highest two megabytes of address space. There are two modes for accessing the DAC. If the G300EN mode bit is low, the chip will assume that a G300 is present. In this case the DAC access is synchronized to the pixel clock to guarantee proper setup and hold times. The DACCS signal will go low followed immediately by the DACWRT signal (for processor write cycles). The DAC cycle will last approximately eight pixel clock cycles with the DACWRT signal going high before the DACCS signal goes high. If the G300EN mode bit is high, the chip will assume that the DAC is not a G300. In this case the DACCS signal is forced low for DAC read cycles, and the DACWRT signal is forced low for DAC write cycles. Again if a VRAM transfer cycle has begun when a DAC access is initiated, the cycle will be held off until the transfer is complete.

DAC accesses may also be held off until horizontal or vertical video blanking intervals if the NOSNOW ENABLE mode bit is high. This prevents DAC access cycles from interfering with the video display. For the NuBus interface the DAC cycle will be held off until a blanking interval occurs. For the SE/30, the BERR

and HALT bus control lines are both driven low which instructs the processor to retry the bus cycle. This prevents a bus time out error from occurring. There is no method of signaling the NuBus to retry the bus cycle, so if the active line time is longer than the NuBus time out period, the NOSNOW ENABLE will have to be written to a low to disable this feature.

The next lower four megabytes of address space are decoded as mode accesses. There are internal mode registers, external mode bits, and external mode read and write control lines (XMODERDB and XMODEWRTB). An address map is included which lists the address map for the specific mode bits.

The bottom eight megabytes are decoded as VRAM space. There are three mode bits that determine the VRAM bank configuration. One, two or four column banks are allowed; and two row banks are allowed which may be either two or four megabytes per bank. Two RAS strobes, four CAS strobes, four write enables and one TROE strobe are generated. VRAM bus cycles are also held off for VRAM transfer cycles. There is also a NuBus block mode transfer enable bit which is valid only for VRAM accesses.

The BUSTYPE input pin is used to select which bus interface will be used. This pin is pulled down on the chip. On the 120 pin package it will be pulled up externally for SE/30 direct slot interfaces, and pulled down for NuBus. On the SE/30 100 pin package it will be pulled up, and on the NuBus 100 pin package it is not available as a pin (it is internally pulled down).

Vertical Blanking Interrupt:
On Macintosh video boards there is an interrupt generated at the video vertical retrace rate. The interrupt is asserted at the beginning of the vertical blanking period and is held until it is cleared out by the interrupt routine in the video driver. The interrupt is cleared out by writing any data to the mode register at address offset A00014 into the slot space. This corresponds to a dummy mode register write.

External Mode Bits:
Four general purpose external mode bits are provided (XEXTMODE(0-3)). These are written to in the same manner as the internal mode bits, but have no internal function. They are intended to be used as pixel depth mode bits, and possibly as video frequency select lines.

There is also a pin called DEBUG which is the output of a four to one multiplexer. The inputs to the mux are TRANSWAITB, DRAM, CYCLE1, and ModesB(3). The first three are signals which may be useful for chip test and debug. ModesB(3) may be used as a general purpose external mode bit. Two other internal mode bits select which of the four signals will go off-chip.

VRAM Transfer Cycles:
There are several different VRAM transfer modes supported.

A programmable number of refresh cycles are performed before each transfer cycle. The number of refresh cycles required per transfer is dependent on the actual transfer cycle frequency which will vary with display resolution, and with the particular transfer cycle mode. Maverick also drives the RAS, CAS, TROE, and DSF signals for the transfer cycle. If a bus cycle is in progress when a transfer cycle request is generated, the bus cycle will complete before the refresh and transfer cycles begin.

If the G300EN bit is low the XTREQ pin is driven from the G300 bus request pin which signals Maverick that it is time to perform a transfer cycle. Maverick will wait until any current bus cycles are complete, and then will assert the XVXAMUXENB signal to signify that the G300 may drive the transfer address. The G300 will then drive the Maverick XTROEIN signal which is used by Maverick to generate the TROE signal for the VRAMs.

If the G300EN bit is high and the Split and Seamless bits are low, then a transfer cycle request will occur with each horizontal sync pulse.

If the G300EN bit is high, the Seamless bit is low and the Split mode bit is high, then the XTREQ input pin is driven from the QSF pin of the VRAMs. In this mode a full transfer cycle is performed at the beginning of each vertical sync, followed by a split transfer at the end of the vertical sync. Then a split transfer will be performed on each transition of the XTREQ pin.

If the G300EN bit is high and the Seamless bit is also high, then Maverick will perform seamless transfers at a rate determined by the TRANSREQ and REQTRANS mode registers. Once a transfer cycle has been performed, the TRANSREQ register is counted down and then another transfer cycle request is performed. Once the transfer cycle request is acknowledged, a programmable number of refresh cycles are performed and the REQTRANS register is counted down. When the refresh cycles are complete, TROE is driven low, and when the REQTRANS count is reached, TROE is driven back high to perform the transfer. At this time the TRANSREQ count is reloaded and the cycle is repeated.

The transfer address for the VRAMs can be generated in Maverick. The transfer address format is determined by three mode bits (see Table 1). The different formats are required to support one or four meg VRAMs, and to provide flexibility in the effective definition of the row x column dimensions. The initial row and column addresses are written into the mode registers. The row address is then incriminated with each transfer cycle provided that the zoom factor is set to zero. For zoom factors other than zero the zoom count will decrement with each transfer and the address will be incriminated when the zoom count reaches zero. The zoom count will then reload and begin counting out the next group of transfer cycles. This allows for a programmable one-dimensional zoom in the 'Y' axis. 'X' axis zoom must be accomplished by pixel replication which will be a function of the pixel clock and shift clock generation circuitry.

Mode Bits				
A5	A4	A3	Row	Column

0	0	0	R0-R8	C0-C8
0	0	1	R1-R9	C0-C7,R0
0	1	0	R2-R10	C0-C6,R0-R1
0	1	1	R3-R11	C0-C5,R0-R2
1	0	0	R0-R7(R8)	C0-C7,(R0)
1	0	1	R1-R8(R9)	C0-C6,R0,(R1)
1	1	0	R2-R9(R10)	C0-C5,R0-R1,(R2)
1	1	1	invalid mode	invalid mode

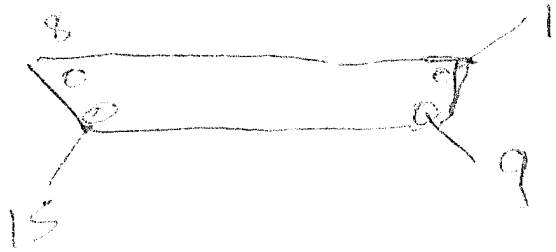
Table 1
Mode bit A5 is intended to be set high for 256K VRAMs. For 256K VRAMs the addresses in ()'s will not be used.

Video Timing Generator:
Video timing signals are generated by counting through a series of mode registers associated with the vertical and horizontal video waveforms. Please refer to the attached drawing for a pictorial description of the timing elements. The horizontal state machine cycles through each element twice per line to allow for equalization pulse generation.

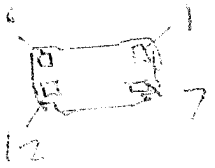
Most of the timing elements will be self-explanatory to those familiar with video timing signals; however, there are some timing elements that are unique to the Maverick design. The FS1 period is used to fill any pipeline that may exist between the VRAM and the DAC. The FS2 period is used to empty the pipeline. NS defines the period where bus access to the DAC will not interfere with the generation of video. HS22 is used for the generation of equalization pulses only.

Interlaced and noninterlaced video formats are supported. Vertical state transitions may be made at half-line or whole- line boundaries. Equalization pulses in the vertical blanking signal may be enabled or disabled. Display sizes up to 2K x 2K are supported. Vertical sync and field ID may be generated externally or internally. For external vertical sync Maverick will wait for an external sync pulse at each vertical front porch period. The falling edge of the active low external sync will force the vertical timing state machine to go into the internal vertical sync state. NTSC timing waveforms are generated by putting the video timing in interlaced mode, selecting the proper horizontal and vertical resolutions, using half line counts in the vertical state machine, and turning on the equalization pulses.

SE/30 Video Cable



1 Black
2 Red1
3 Brown
4 N/C
5 Green
6 Black
7 N/C
8 N/C
9 Yellow
10 Red2
11 Black
12 Orange
13 Black
14 Black
15 White ~~/ Red~~



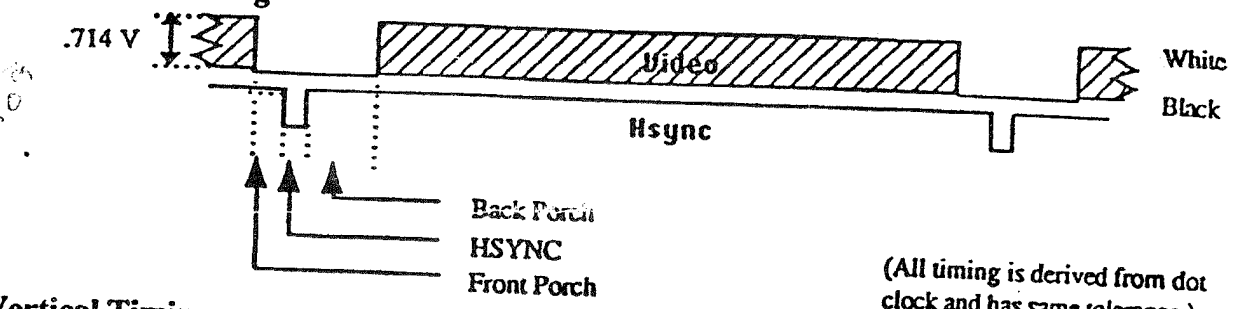
1 Red2
2 Yellow
3 Green
4 Red1
5 Brown
6 Orange
7 N/C
8 Black
9 Black
10 Black
11 Black
12 White / Red

PRELIMINARY SPEC

16" MONITO

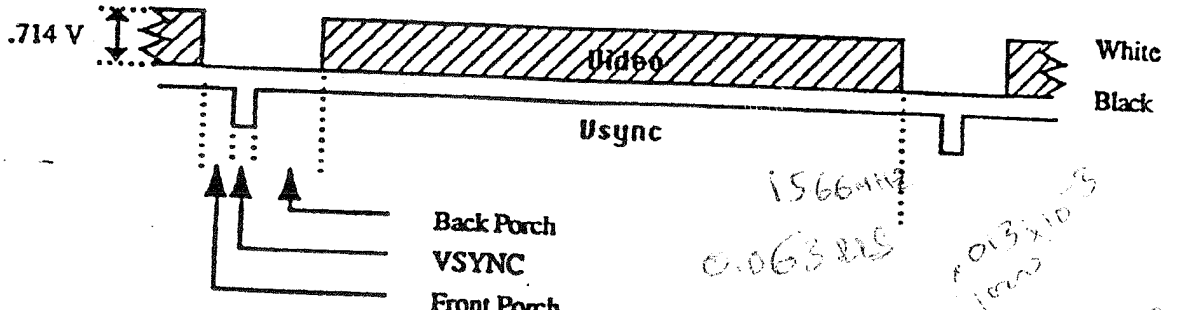
5.1 Input signal timing

Horizontal Timing



(All timing is derived from dot clock and has same tolerance.)

Vertical Timing



active pixels per line	832	active # of lines	624
interlace ratio	1.00	vertical refresh (Hz)	75.00
vertical blank lines	30.00	Total lines	654.00
		line time (us)	20.39
vertical front porch (lines)	1	vertical blanking time (us)	611.62
vertical sync (lines)	3	time (us)	61.16
vertical back porch (lines)	24	time (us)	61.16
		Total V retrace	489.30
Horiz blank words	18	Horiz blank pixels	550.46
		Horiz blank words	288
		Horiz blanking time (us)	18.00
		Horiz frequency (Hz)	5.24
H front porch words	2	H front porch pixels	49,050.00
H sync words	4	H sync pixels	32.00
H back porch words	12	H back porch pixels	64.00
		H front porch time (ns)	192.00
		H sync time (ns)	582.50
		H back porch time (ns)	1,164.99
		Total H retrace	3,494.98
		words / line	4,659.97
pixel frequency (Hz)	54,936,000	time / word (ns)	70.00
		pixel time (ns)	291.25
			18.20

APPLE CONFIDENTIAL

ICS PART NUMBER (Status)	ICS1494-536 (In Prod)
1394 Equiv	
CUSTOMER	MICRON TECH 20-0319
COMPATIBLE VGA CHIPSET	

ADDRESS LOCATION (Hex)	OUTPUT FREQUENCY (MHz)
00	
01	30.240
02	15.667
03	17.234
04	12.273
05	57.283
06	80.000
07	100.000
	EXTFREQ
08	
09	20.000
0A	25.175
0B	28.322
0C	31.320
0D	34.000
0E	36.000
0F	38.000
	40.000
10	
11	44.900
12	48.000
13	50.350
14	54.000
15	60.000
16	65.000
17	70.000
	75.000
18	
19	85.000
1A	90.000
1B	95.000
1C	105.000
1D	110.000
1E	115.000
1F	120.000
	125.000

NOTES: All patterns tagged *STD* are s
be considered as custom patterns, not

MAVERICK MEMORY MAP AND MODE REGISTER DESCRIPTIONS

RAM	Mode A	Mode B/External Modes	DAC	ROM
Fs00 0000 - Fs7F FFFF	Fs80 0000 - Fs9F 0000	FsA0 0000 - FsBF FFFF	FsC0 0000 - FsDF FFFF	FsE0 0000 - FsFF FFFF

Register Address	Contents	Bit #	Function
Fs800000	Horiz Front Porch	0-6	Horizontal Front Porch Interval
Fs800004	HSync/2	0-5	Half of the Horizontal Sync pulse width
Fs800008	Horiz Back Porch	0-10	Horizontal back porch interval - NS
Fs80000C	Line/2 (HLINE)	0-10	[# of visible pixels - (FS1 + FS2)] / 2
Fs800010	Vert Front Porch	0-4	Vertical front porch interval
Fs800014	Vert Sync	0-6	Vertical sync interval
Fs800018	Vert Back Porch	0-10	Vetical back porch interval
Fs80001C	Lines/Frame	0-10	Number of visible lines per frame or field
Fs800020	HSync22	0-10	FS1 + FS2 + NS + Horiz Front Porch + Horiz back porch + Line/2
Fs800024	Row MSBs	0-10	Row transfer address MSBs
Fs800028	Row LSB	9	Row transfer address LSB
Fs800028	Col / Row LSB	0-8	Column transfer address
Fs80002C	Mode Reg A	0	Equalization pulse Disable (1 = no equalization pulses)
Fs80002C	Mode Reg A	1	Interlace mode enable
Fs80002C	Mode Reg A	2	External Sync Mode Disable (0 = external sync mode)
Fs80002C	Mode Reg A	3,4,5	ROW/COL transfer address format
Fs80002C	Mode Reg A	6	spare
Fs80002C	Mode Reg A	7	G300 Disable (0 = G300 ENABLED)
Fs80002C	Mode Reg A	8,9	Number of Column banks (0 = 1 bank, ..., 3 = 4 banks)
Fs80002C	Mode Reg A	10	Vertical count by wholelines
Fs800030	FS1	0-5	Format run pipe fill
Fs800034	FS2	0-5	Format run off
Fs800038	Req to Trans Dly	0-10	Seamless transfer request to transfer delay count
Fs80003C	Trans to Req Dly	0-10	Seamless transfer to next request count
FsA00000	External Mode	0-3	External mode bits that go off chip
FsA00004	Refresh Count	0-4	Transfer cycle start to transfer cycle delay for refresh cycles
FsA00008	Mode Reg B	0-8	video on | Interrupts on | NuBus block mode transfer enable | Debug D3 | 2 or 4 meg Row banks |
FsA00008	Mode Reg B		NoSnow Enable | Seamless | VRAM Split transfers | FIDsel | DebugSel (2) |
FsA00008	Mode Reg B	0	Video timing enable
FsA00008	Mode Reg B	1	Interupt enable
FsA00008	Mode Reg B	2	NuBus Block Transfer enable
FsA00008	Mode Reg B	3	Debug data
FsA00008	Mode Reg B	4	Row bank size (0 = 2meg, 1 = 4meg)
FsA00008	Mode Reg B	5	No Snow enable
FsA00008	Mode Reg B	6	Seamless
FsA00008	Mode Reg B	7	Split
FsA00008	Mode Reg B	8	FIDsel
FsA00008	Mode Reg B	9,10	DebugSel (0 = TRANSWAITB, 1 = DRAM, 2 = CYCLE1, 3 = Debug data)
FsA0000C	Zoom	0-4	Zoom factor
FsA00010	NS	0-7	Period in Horizontal back porch interval to begin holding off DAC accesses to prevent screen 'snow'
FsA00014	Interrupt Clear	X	This address is written to for clearing the interrupts
FsA00018			
FsA0001C			
FsA00020	External		
FsA00024	External		
FsA00028	External		
FsA0002C	External		
FsA00030	External		
FsA00034	External		
FsA00038	External		
FsA0003C	External		

31.625 MHz

31 x 10^-9

(0.031 µs)

20.55

- 2.03