PowerPC™

# Long Trail: The PowerPC Platform for MacOS and Beyond

March 1997

IBM

# Agenda

- PowerPC Platform
- Long Trail Hardware
  - CPU Bus
  - North Bridge Chip set
  - PCI Bus
  - South Bridge
  - ISA Bus
  - Physical Design
- Long Trail Software
  - Firmware
  - Operating Systems
- Long Trail Product Opportunities
- IBM Microelectronics Support

- The agenda today includes a brief overview of the PowerPC Platform objectives, a step by step decription of the Long Trail reference design hardware and software, the Long Trail product opportunities, plus a look at the IBM Microelectronics design support available.

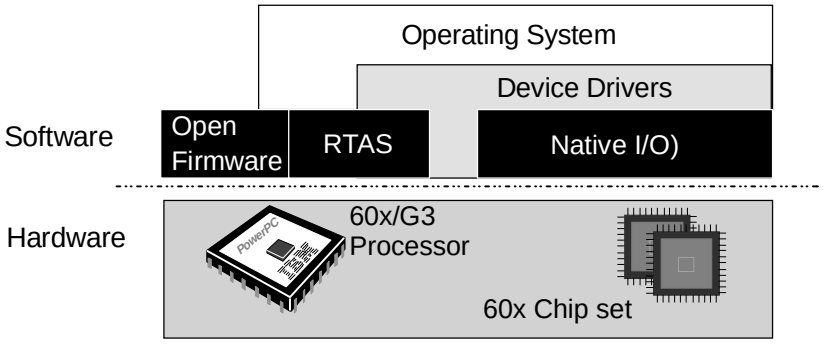
## PowerPC Platform Architecture

- Developed by Apple Computer, IBM and Motorola
- Primary goal is to define an open architecture and minimum system requirements for development of PowerPC based computer systems
  - Incorporate multi-operating systems
  - Broad enough to cover portables through server platforms in single and multiprocessor configurations
  - Leverage existing and future industry-standard buses and interfaces
  - Provide flexible address map
  - Build upon Open Firmware boot environment

- The PowerPC Platform (PPCP) specification defines a system architecture developed by Apple, IBM, and Motorola. Based on the PowerPC microprocessor, this architecture, formerly known as the Common Hardware reference Platform (CHRP), defines an open architecture and minimum system requirements for a PowerPC based computer. This architecture can incorporate muti-operating systems and is broad enough to cover portables through server platforms in single and multiprocessor configurations. Further, it leverages existing and future industry-standard buses and interfaces. PPCP builds upon the Open Firmware boot environment which allows multiple operating systems, including Apple's Macintosh OS (MacOS), independent of a specific hardware implementation.

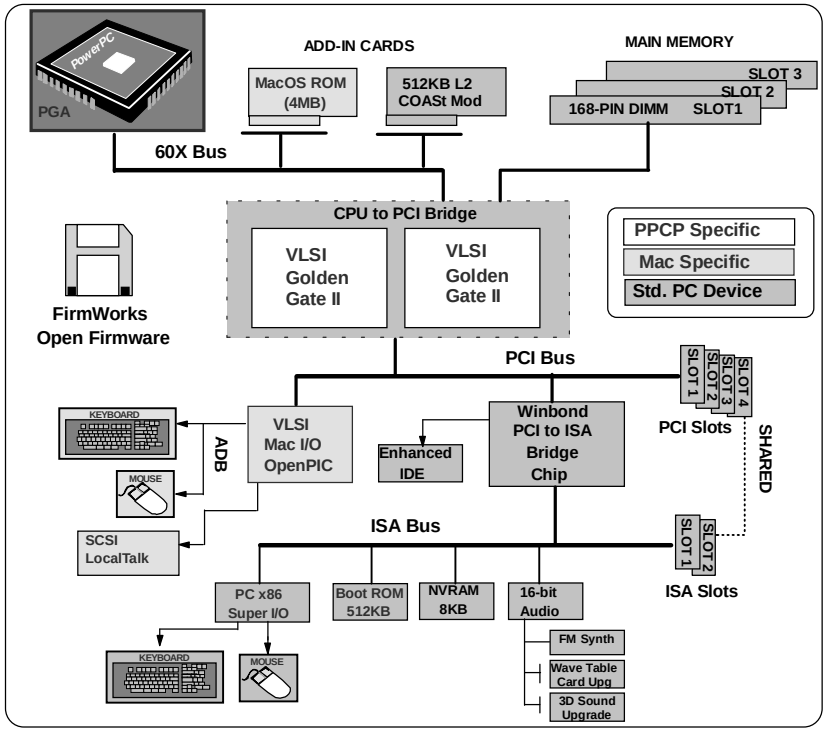
# PowerPC Platform Architecture

- PPCP defines an open architecture
- Open Firmware complies with IEEE Standard 1275-1994
- Open Firmware (Boot, RTAS, and Device Drivers) acts as an insulation layer between the OS and a specific hardware implementation

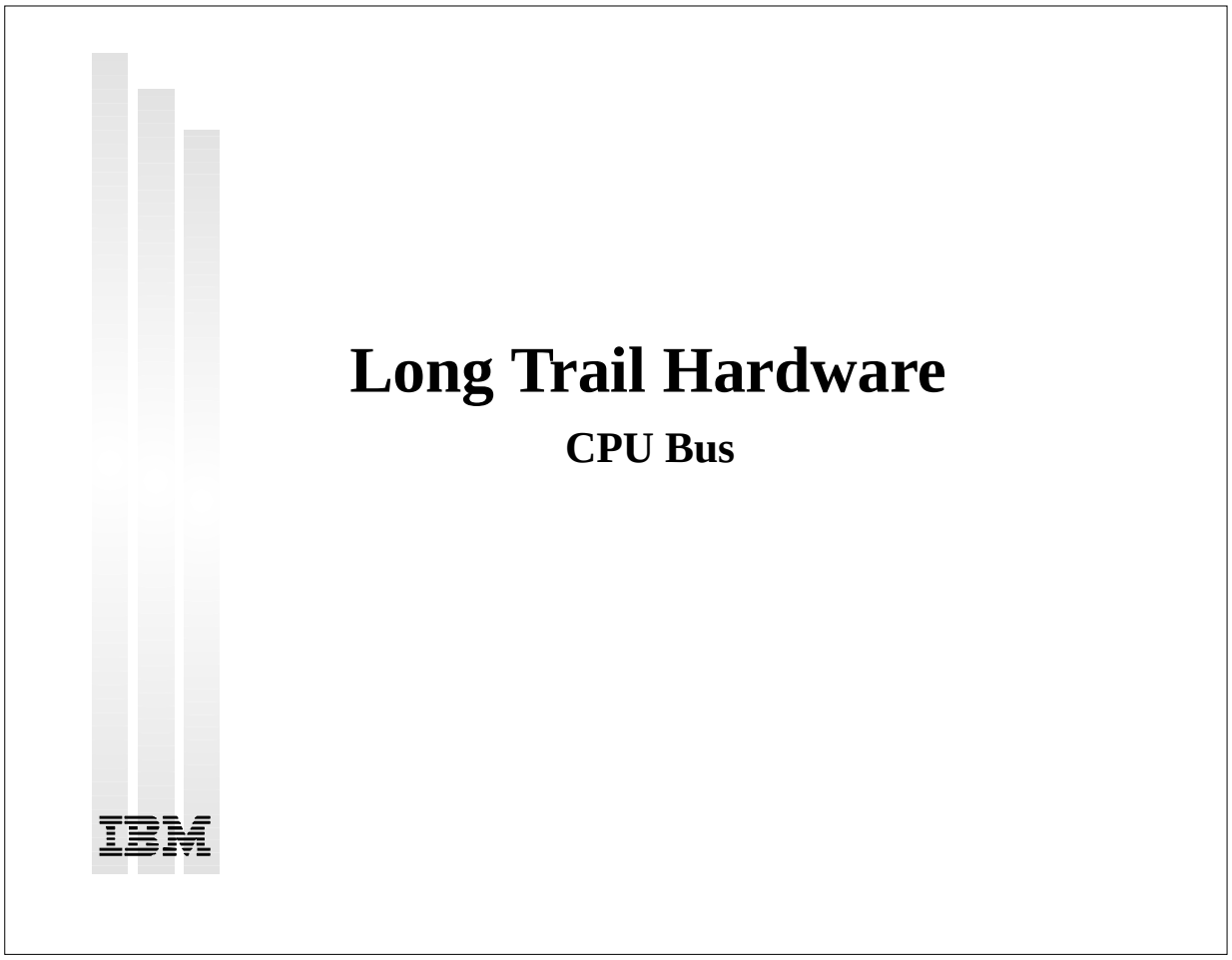



- Much of the hardware independence of the PPCP architecture is accomplished by the use of Open Firmware. Open Firmware is boot, Run Time Abstraction Software (RTAS), and device driver code that complies with IEEE Standard 1275-1994, a non-proprietary international standard. Open Firmware is easily portable between hardware platforms.
- After boot, RTAS provides a specific interface to common operating system functions, such as: NVRAM use and access, real time clock, and power management.
- To be PPCP compliant, operating systems will standardize native I/O software interfaces.

# Long Trail Reference Design



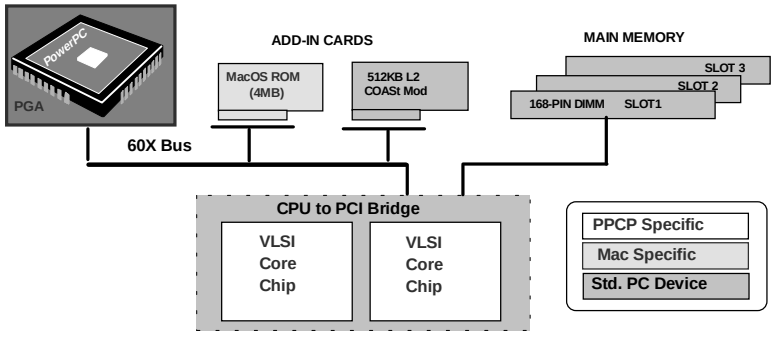

- Long Trail is the first IBM reference design based on the PPCP architecture. As indicated in this chart, the majority of components are standard PC devices.
- The ultimate goal of the Long Trail design is to complete the core motherboard, chip set, and software development, in order to shorten OEM customer product time to market. This, in turn, will broaden the PowerPC microprocessor market segment. Toward this goal, IBM has formed relationships with third party industry suppliers such as VLSI Technology for the core chip set and FirmWorks for the Open Firmware.




- We will begin our look at the details of Long Trail hardware with the CPU bus.

# CPU Bus - Overview

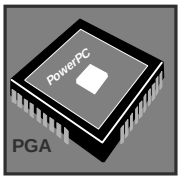
- Four devices connected to 60X bus
  - PowerPC CPU
  - COASt L2 Cache module
  - MacROM module
  - Golden Gate II chip set




- Four major devices are connected to the PowerPC 60X CPU bus. They are: PowerPC CPU, COASt level two cache module, Apple Toolbox ROM (also referred to as the MacROM), and the Golden Gate II chip set.

# CPU

- PowerPC Microprocessor
  - 32b address, 64b data, & control signals
  - 603e/ev, 604e/e2, 32-bit advanced G3 processors supported
- One 288-pin (17x17) ZIF PGA Socket on board
- Accommodate 604e or 603e:
  - 604e/e2 up to 233MHz available today
  - 603e/ev up to 225MHz available today




- Configurable CPU Speed and Bus Mode via on-board jumpers
- Modes selectable
  - Normal
  - Fast-L2 (Data Streaming)
  - No-DRTRY
- RISCWatch interface on board for engineering debug
- Voltage Regulator Module (VRM)

- Long Trail supports the current 603e/ev, 604e/e2 PowerPC processors. Additionally, the CPU can be upgraded to the 32-bit members of the advanced G3 family of processors. The CPU is upgraded via an industry standard 288-pin Pin Grid Array (PGA), Zero Insertion Force (ZIF) socket. The design will accommodate all current processors, as well as planned G3 processors. The CPU speed and bus mode are configurable with on-board jumpers. All three PowerPC bus modes are supported: Normal, Fast-L2, and No Data Retry. A RISCWatch connector is included for engineering debug. The CPU is powered via a 40-pin Voltage Regulation Module (VRM).

# Voltage Regulator Module

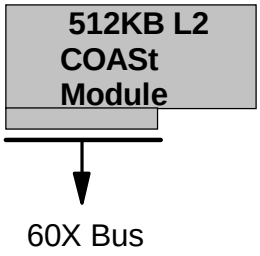
- Used Industry Standard VRM
- VRM vendors: VXI, Semtech, Celestica, Astec, Linfinity, Raytheon & Cherry Semi.
- VRM specs (varies w/ different vendors)
  - Input voltages: 5V +/-5% & 12V +/-5%
  - Output voltages: 1.3 - 3.5V
  - Currents: 0.8A - 13A, dI/dt <= .1A/uS
  - Slew Rate: 30A/uS
- Connector: 40-pin AMP socket (part# 532955-7)
- Solutions can be embedded on motherboard for cost reduction components supplied from: Semtech, Micro Linear, Linear Technology, National Semiconductor and Unitrode Integrated Circuit, among others

| 5 | 4 | 3 | 2 | 1 | VCC (V) |
|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1.30 |
| 0 | 1 | 1 | 1 | 0 | 1.35 |
| 0 | 1 | 1 | 0 | 1 | 1.40 |
| 0 | 1 | 1 | 0 | 0 | 1.45 |
| 0 | 1 | 0 | 1 | 1 | 1.50 |
| 0 | 1 | 0 | 1 | 0 | 1.55 |
| 0 | 1 | 0 | 0 | 1 | 1.60 |
| 0 | 1 | 0 | 0 | 0 | 1.65 |
| 0 | 0 | 1 | 1 | 1 | 1.70 |
| 0 | 0 | 1 | 1 | 0 | 1.75 |
| 0 | 0 | 1 | 0 | 1 | 1.80 |
| 0 | 0 | 1 | 0 | 0 | 1.85 |
| 0 | 0 | 0 | 1 | 1 | 1.90 |
| 0 | 0 | 0 | 1 | 0 | 1.95 |
| 0 | 0 | 0 | 0 | 1 | 2.00 |
| 0 | 0 | 0 | 0 | 0 | 2.05 |
| 1 | 1 | 1 | 1 | 1 | NO CPU |
| 1 | 1 | 1 | 1 | 0 | 2.10 |
| 1 | 1 | 1 | 0 | 1 | 2.20 |
| 1 | 1 | 1 | 0 | 0 | 2.30 |
| 1 | 1 | 0 | 1 | 1 | 2.40 |
| 1 | 1 | 0 | 1 | 0 | 2.50 |
| 1 | 1 | 0 | 0 | 1 | 2.60 |
| 1 | 1 | 0 | 0 | 0 | 2.70 |
| 1 | 0 | 1 | 1 | 1 | 2.80 |
| 1 | 0 | 1 | 1 | 0 | 2.90 |
| 1 | 0 | 1 | 0 | 1 | 3.00 |
| 1 | 0 | 1 | 0 | 0 | 3.10 |
| 1 | 0 | 0 | 1 | 1 | 3.20 |
| 1 | 0 | 0 | 1 | 0 | 3.30 |
| 1 | 0 | 0 | 0 | 1 | 3.40 |
| 1 | 0 | 0 | 0 | 0 | 3.50 |

- The Voltage Regulation Module is the industry standard type used for x86 designs. Many vendors offer this off-the-shelf part.
- In the Long Trail design, core processor voltage is easily selectable from 1.30 to 3.5 volts using a 5-bit input. This provides great flexibility for any specific microprocessor application conditions. The 5-bit input also provides the wide voltage range necessary to support current and extremely low power G3 processors.
- For possible cost reduction, a regulation solution could be embedded on the motherboard with components from a variety of suppliers.

# COASt L2 Cache Module

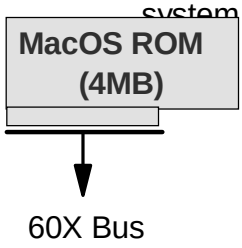
- Using 160-pin L2 COASt 3.1 modules
- Pipelined-Burst configuration
- 512KB size
- Pin #114, BOSEL, should be tied low for linear burst
- Cacheable Memory up to 512MB
- Vendors: Corsair, Paradigm, Samsung, etc.....




- Also on the 60X bus is an industry standard 160-pin level two cache connector. Widely available 512KB pipelined burst Cache On A Stick (COASt) modules can be utilized.
- Pin number 114 of the cache interface is tied low to provide the necessary linear burst for PowerPC and Cyrix processors. Using an 11-bit tag, up to 512MB of main memory can be cached. COASt modules are offered by all major cache suppliers.

# Mac ROM DIMM

- Provided on a 160-pin DIMM card
- 3.3V, 4MB Flash or Mask ROM to contain "Toolbox" for MacOS. Development uses FlashROM and production uses MaskROM.
- IBM designed ROM built by Anthem, Inc. -- electronic card vendor using AMD AM29LV800T-120SC flash ROM.
- Sharp, Hitachi & Samsung are the tentative ROM vendors. Apple will choose strategic ROM vendors.
- Apple allows licensees to buy ROM chips which can be populated on the motherboard for cost reduction
- MacROM contains significant portion of MacOS and is accessed frequently during operation.

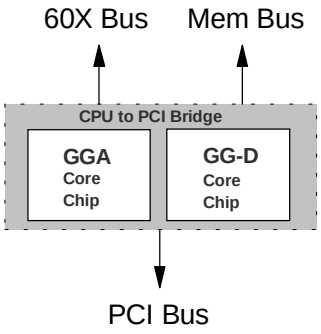



- Rounding out the 60X bus is a 3.3 volt 160-pin connector for the 4MB MacOS Toolbox ROM, MacROM. Flash ROM is used for development and mask ROM for production. IBM designed the first 3.3V MacROM which is available from Anthem, Inc., an electronic card vendor using the AMD AM29Lv800T-120SC flash ROM part. Several other major ROM suppliers are producing prototype parts. Apple will choose the strategic flash and mask ROM suppliers. Apple does allow licenses to buy ROM chips which can be populated on the motherboard to reduce cost. The MacROM contains a significant portion of the MacOS and is accessed frequently during system operation.


- The next topic is a closer look at the VLSI Golden Gate II north bridge chip set

# VLSI Golden Gate - Overview

- Features include:
  - PowerPC Platform (CHRP) memory map
  - Multiple functions integrated:
    - PowerPC-to-PCI bridge
    - 60x bus arbitor/bus support
    - L2 cache controller
    - DRAM controller
    - ROM controller
- Two-chip solution from VLSI:
  - GG-A (Control + Address path): 240 MQFP (VLSI p/n VAS96011)
  - GG-D (Data path): 208 MQFP (VLSI p/n VAS96012)
- Integrated buffers for PCI/DRAM access
- 0.5 micron technology
- 3.3V power supply




- The two-chip high-performance VLSI Golden Gate II core logic incorporates a PowerPC 60X bus-to-PCI bridge, a 60X bus arbiter and advanced bus support, a L2 cache controller, a DRAM controller, and a ROM controller. The first chip, GG-A, contains all the controls, the address path and the PCI data path in a 240-pin MQFP package. The second, GG-D, is a three-way, 64-bit data path chip that contains the 60X bus to the DRAM and to GG-A in a 208-pin MQFP package. The chip set contains integrated buffers for faster PCI bus and DRAM access. Both chips are 0.5 micron, 3.3V technology.

# Golden Gate - 60X Bus Support

- 60x arbiter integrated
  - Can support up to 2 processors
  - Can be disabled to use external arbiter
  - Long Trail configuration (via Power-on Strapping):
    - enable the arbiter in GG-A
    - configured as HB #0
- Work as either a slave or master device on 60X bus
  - Slave: responds transactions initiated by CPU
  - Master: performs snoop push for L2 cache
- Supported pipelined access
  - Pipeline enabled normally
  - Can be disabled for debugging purpose

- The integrated 60X bus arbiter can support up to 2 processors. This arbiter can be disabled if the use of an external arbiter is necessary. Long Trail does enable the arbiter, located in GG-A, via power-on strapping. It is configured as Host Bridge (HB) number 0. The chip set can work as either a slave or master device on the 60X bus. As a slave, it responds to CPU initiated transactions. As a master, it can perform a snoop push for the L2 cache. Advanced pipelined access is a base function, but can be disabled for debugging purposes.

# Golden Gate - L2 Cache Interface

- GG has an integrated L2 cache controller:
  - Look aside and direct map
  - Supports write-through or write-back (aka. copy-back) mode
  - Size can be 256K, 512K, or 1MB (not COASt supported)
- With integrated TAG comparator, can support cache with 8 or 11-bit tags
  - TAG0 is dedicated as the DIRTY bit

- Another major integrated function is the L2 cache controller. It is look-aside and direct mapped. Write-back (aka. copy-back and write-through modes are supported with available cache sizes of 256KB, 512KB, and 1MB. A 1MB cache size is not currently supported by the COASt specification. However, cache could be put down on the motherboard outside of the COASt specification. Due to the integrated tag comparator, 8 or 11-bit tag modules can be used. Because TAG0 is dedicated as the dirty bit, 11-bit modules are recommended to increase the amount of cached memory.

# Golden Gate - DRAM Interface

- Support multiple types of DRAM
  - FPM, EDO, Burst EDO, Synchronous
- Three 168-pin JEDEC Standard 3.3v non-buffered DIMM
  - Each slot can support 2 banks
  - Slot 1-3 can be installed with FPM, EDO,or BEDO DIMM
  - Only slot 1-2 can be installed with SDRAM
- Memory Organization:
  - Up to 6 non-interleaved banks for FPM, EDO, and B-EDO
    - Maximum Memory = 192MB (16Mb) or 768MB (64Mb)
  - Up to 4 non-interleaved banks for SDRAM
    - Maximum Memory - 128MB (16Mb) or 512MB (64Mb)

- Main memory is on a dedicated bus from Golden Gate. Fast Page Mode (FPM), Extended Data Out (EDO), Burst EDO, and SDRAM type DIMMs are supported. The modules conform to the 168-pin 3.3V non-buffered JEDEC standard. Long Trial contains three memory upgrade slots. Up to six non-interleaved banks of FPM, EDO, and Burst EDO can be used resulting in 192MB maximum memory using 16Mb technology chips or 768MB maximum using 64Mb chips. Or, four non-interleaved banks of SDRAM can be utilized which yields 128MB total, using 16M-bit technology or 512MB, using 64M-bit technology components.

# Golden Gate - DRAM Interface

- Buffer extensive design:
  - 1 write buffer (32B FIFO) dedicated to PowePC master
  - 1 write buffer (32B FIFO) dedicated to PCI master
- Firmware requires EEPROM on each DIMM module to report memory information:
  - presence, type, speed... etc
  - EEPROM address 1/2/3 are assigned to slot 1/2/3 respectively
  - I2C interface is implemented in Macintosh I/O chip

- The Golden Gate DRAM interface contains PowerPC and PCI master write buffers for performance. The JEDEC standard requires an EEPROM on each DIMM module to report memory information, such as: presence, type, speed, and configuration. The I2C interface is implemented in the Macintosh I/O chip.

# Golden Gate - ROM Interface

- ROM support is configurable
  - can be 8/16/32/64-bit wide
  - two independent banks
  - selected by setting strap pins or register pins
  - 64-bit burst read and cached ROM cycles
- Golden Gate - bank 0 & bank 1
  - Bank 0 is used for MacROM
  - Bank 1 is used for PCI boot ROM
- Support FlashROM programming
  - normally no write to ROM allowed; if violated GGII will generate a machine check exception
  - ROM_WE bit must be active to write Flash
- Long Trail uses ROM bank 0 for MacROM, disables ROM bank 1 (ISA bus boot)

- The integrated ROM interface controller supports two independent 8-, 16-,32-, or 64-bit wide banks. ROM accesses can be redirected to the PCI bus for boot purposes. In addition, 64-bit burst read and cached ROM cycles are able to provide high system initialization access performance, a clear advantage for the required MacROM operation. Bank 0 is used for the MacROM, while Bank 1 is used for a PCI boot ROM, if implemented. Flash ROM reprogramming is supported. If the ROM write enable bit is not active, the GGII chip set will generate a machine check exception for protection. Long Trail designates Bank 0 for the 64-bit MacROM and disables ROM Bank 1.

# Golden Gate - PCI Bus Interface

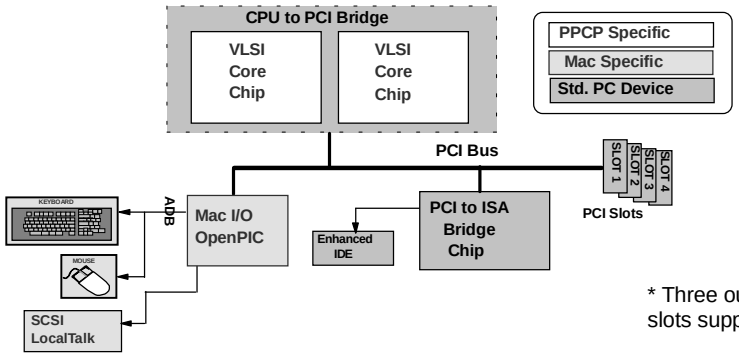
- PCI 2.1 compliant
- Synchronous or asynchronous mode
  - Synchronous at 1/2 of CPU clock
  - Selected via Power-on strapping
- Multiple functions supported:
  - Concurrent operation of 60X bus and PCI bus
  - Write combining/merging of PowerPC-to-PCI writes
  - Big- and little-endian mode
- Single load; 3.3V signaling level; 5V-tolerant PCI pads

- Golden Gate II is PCI 2.1 compliant. Synchronous and asynchronous 60X to PCI bus operation are supported. The synchronous mode maintains the PCI bus at one half of the 60X bus speed. The PCI and 60X bus can operate concurrently. Merging of PowerPC-to-PCI writes increases bus efficiency. To allow for different operating systems, big and little-endian protocol are supported. Golden Gate II presents a single load to the PCI bus.


- Now we can step through each item located on the PCI bus.

# Long Trail - PCI Bus

- Three devices, four expansion slots on PCI bus:
  - CPU to PCI bridge (GG-A) chip
  - Macintosh I/O chip
  - PCI-ISA bridge chip
  - 4 PCI expansion slots *

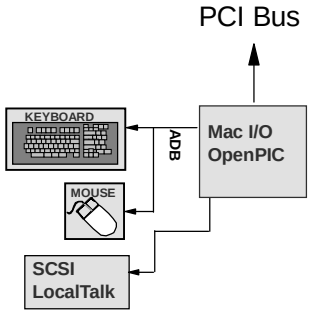



* Three out of four expansion slots support PCI bus master

- Three devices plus four expansion slots reside on the Long Trail PCI bus. The three devices include the GG-A core logic chip, a Macintosh I/O chip, and a PCI-to-ISA bridge chip. Three of the four PCI expansion slots may be used for a bus master device.

# Long Trail - Mac I/O

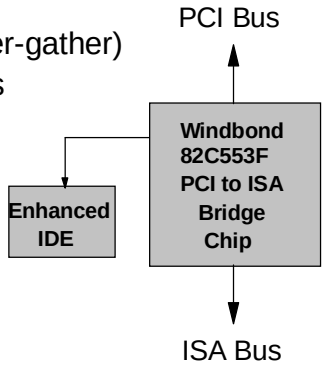
- Mac I/O chip contains system Multi-Processor Interrupt Controller, MPIC
- Traditional Macintosh I/O including:
  - ADB for keyboard and mouse
  - MESH SCSI for hard drive, CD-ROM, legacy printers
  - SCC controller for LocalTalk ports (2 channels)
- DBDMA functions
- Integrated VIA: an operating system timer.
- PCI arbitration, not used in LT design
- A 2-wire I2C interface to detect DIMM ID
- Marketed with GGII from VLSI, named Pier 39 (VLSI p/n VAS96013)




- The Macintosh I/O chip contains the system Multi-Processor Interrupt Controller (MPIC), also referred to as OpenPIC. All traditional Macintosh I/O function is supported, including: Apple Desktop Bus (ADB) for keyboard and mouse interface, MESH SCSI for external hard drive, CD-ROM, legacy printer support, and SCC ports for Local Talk. Macintosh Desktop Bus Direct Memory Access, or DBDMA, and an operating system timer, called VIA, are also resident in this chip. Although it is not used by the Long Trail design, the Mac I/O chip can perform PCI arbitration. Finally, it also includes an I2C interface to detect DRAM identification information. This chip will be marketed by VLSI with GGII under the name of Pier 39.

# Long Trail - PCI-ISA Bridge

- Winbond 82C553F (208-pin, MQFP)
- Used in PowerPC and x86 designs
- PCI 2.1 compliant
- Dual channel PCI bus master eIDE
- Up to 33MHz PCI bus operation
- Additional Function:
  - Two 82C37A DMA controllers (scatter-gather)
  - Two 82C59A ISA interrupt controllers
  - 8254 Timer
  - PCI Arbiter
  - Boot ROM control

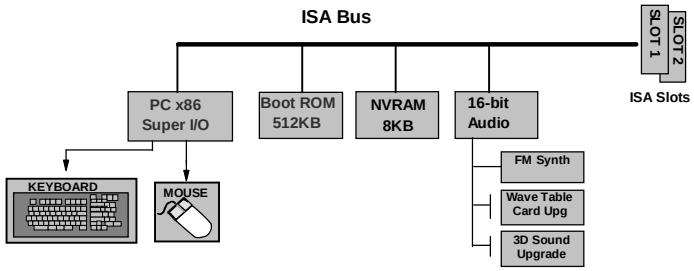



- The PCI to ISA bridge is provided by Winbond, Inc. in a 208-pin MQFP package. The chip is used in x86 and PowerPC designs. It is PCI 2.1 compliant and support both x86 and PowerPC modes of operation. This chip has an integrated dual channel PCI bus master enhanced IDE (eIDE) controller for up to four peripherals. Long Trail is designed to operate using a internal eIDE drive. The PCI interface supports up to 33MHz operation. Additional ISA bridge chip function includes two enhanced, seven-channel 82C37A 32-bit DMA controllers with scatter-gather capability, two 82C59A ISA interrupt controllers and a 8254 timer. The embedded PCI arbiter supports CPU, IDE, ISA and five additional bus masters. For the Long Trail design, boot ROM control is accomplished with this chip.


- We can now cover the ISA bus.

# Long Trail - ISA Bus

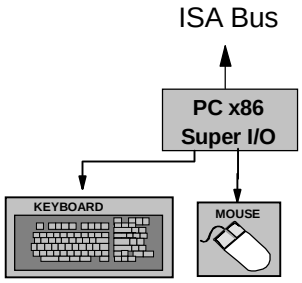
- Five devices, two expansion slots on ISA bus:
  - PCI-ISA bridge chip
  - Super I/O chip
  - Boot ROM
  - NVRAM
  - 16-bit Audio




- Five PC standard devices reside on the Long Trail ISA bus. They include: the Winbond PCI-to-ISA bridge chip, a Super I/O chip, the system boot ROM, NVRAM, and a 16-bit audio controller. Also, two 16-bit ISA slots are available for expansion.

# Long Trail - Super I/O

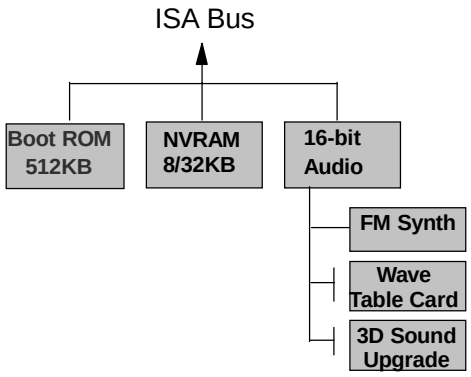
- National Semiconductor PC87307VUL
- Provides the following:
  - Real Time Clock
  - Two PC16C550 Uarts serial ports
  - PC8477 Floppy Disk Controller
  - An IEEE 1284 EPP/ECP parallel port
  - 16 GPIOs
  - Infrared interface (not MacOS supported)
  - PC keyboard & mouse controller
- NS supports Phoenix, IBM & AMI codes




- A National Semiconductor 307 chip is used for super I/O. It includes the system Real Time Clock (RTC), two PC16C550 Uarts serial ports, a PC8477 floppy disk controller, an IEEE 1284 EPP/ECP parallel port, 16 general purpose I/O registers, an infrared interface (not currently supported in MacOS), and PC mouse and keyboard controllers. The chip supports keyboard code from Phoenix, IBM and AMI.

# Long Trail - Other ISA Devices

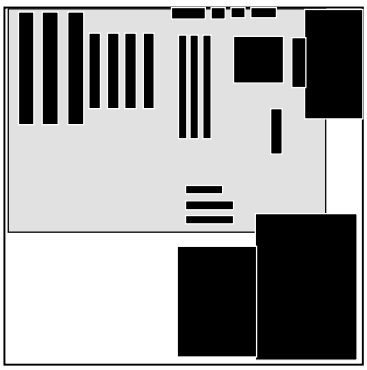
- Boot ROM
  - 512KBx8 FlashROM
  - Open Firmware (w/RTAS) Code
  - Flash update with lock
- NVRAM
  - 8K or 32KB x8 chips used
- Audio
  - Crystal CS4236 16-bit controller
  - Integrated FM synthesis
  - Wave Table upgrade connector
  - 3D Audio upgrade connector




- The remainder of the ISA bus includes: a flash programmable 512KBx8 boot ROM, 8 or 32KBx8 of NVRAM, and the 16-bit Crystal 4236 audio controller with integrated FM synthesis. The audio can also be upgraded via wave table and 3D sound add-in cardlets.

# Long Trail - Layout

- ATX
  - Open Specification, PC Industry Standard
  - Basically a STD BABY-AT Layout Rotated 90 Degrees
  - Processor Shifted Away From Expansion Slots - No Full Size Adapter Card Conflict
  - 2X High Rear I/O Aperture
  - Optimized Power Supplies
  - External Fan for Processor Cooling
  - Overall Dimensions = 9.6" X 12"
- Physical Design
  - 4-layer, 2S2P
  - PC Industry Standard components
  - PGA CPU Upgrade

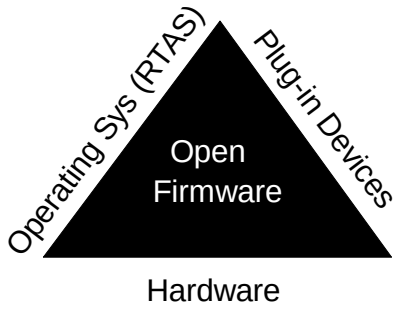


- The Long Trail layout is based on the industry standard ATX form factor which is an open specification. ATX is an evolution of the popular Baby-AT form-factor. By rotating it 90-degrees, the processor is shifted away form the expansion slots, thus eliminating any conflict with full size adapter cards. This rotation also locates the microprocessor in proximity of the power supply. New ATX power supplies have external fans for processor cooling and improved chassis air flow. Long Trail includes a double height rear aperture that permits usage of both x86 and Macintosh style I/O. The overall dimension of motherboard is 9.6"x12".
- The ATX form factor was one in many customer design input requests, others include: a 4-layer, 2S2P design, use of PGA CPUs, and using PC I industry standard components like the COASt L2 and voltage regulation modules.

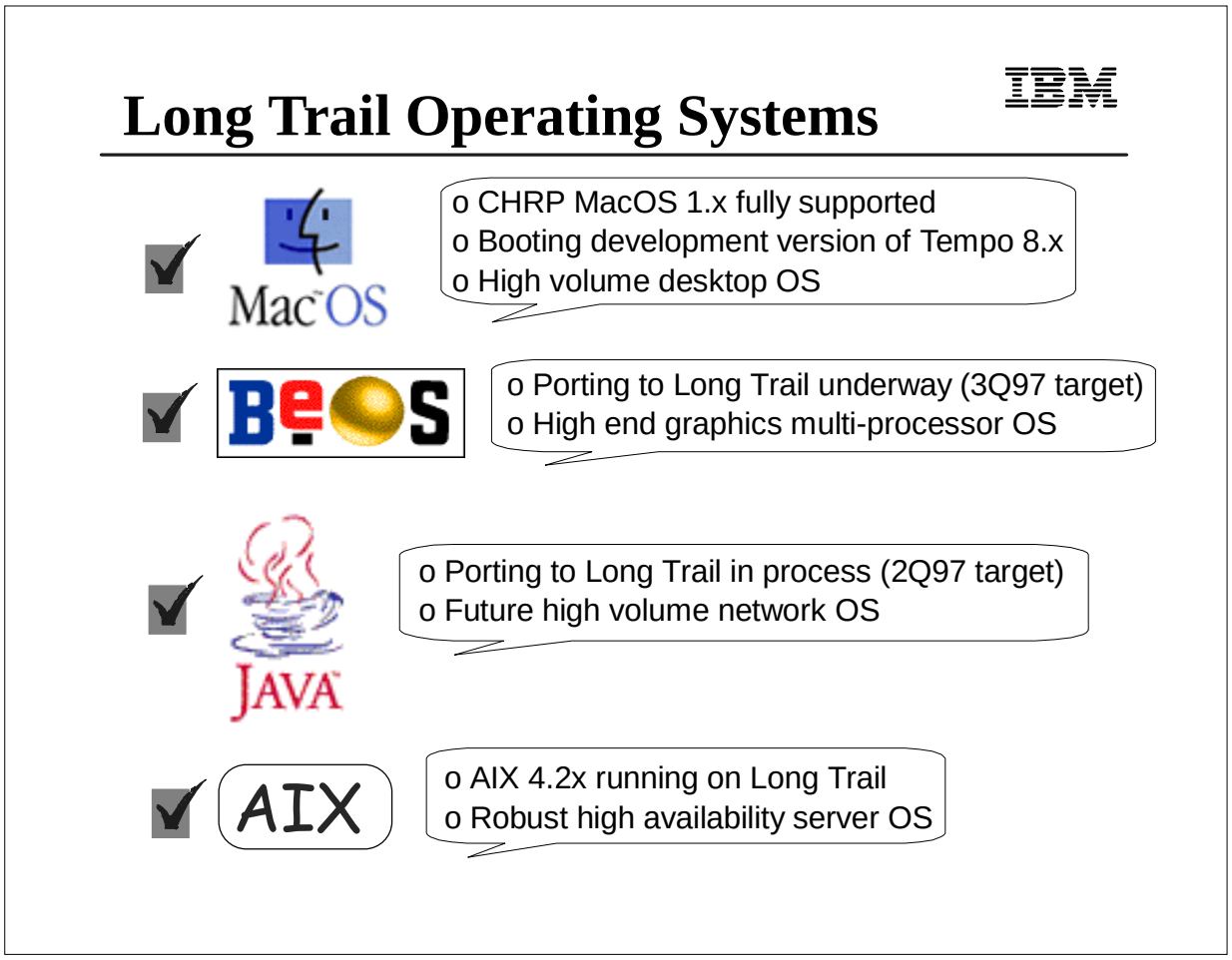

- Now that we have discussed the hardware in detail, we can cover an overview of the Long Trail system software.

# FirmWorks Open Firmware

- Founded in 1994 by Mitch Bradley -- initial developer of Open Firmware
- Support for system ROM, device drivers, training, and specialized programming
- Power Firmware Features:
  - Operating System Multi-Boot
  - Plug-In Drivers
  - Interactive Forth Debugger
  - Configuration Maintenance
  - Client Interface (boot config)
  - GUI Toolkit
  - Flash Update Utility (boot/MacROM)




- FirmWorks was founded in 1994 by Mitch Bradley, who invented Open Firmware. FirmWorks will support development of system ROMs and device drivers. They also offer training and specialized programming in support of their products. FirmWorks Power Firmware includes the following functionality: operating system multi-boot to allow one firmware version for multiple operating systems, plug-in drivers to auto-detect many of the commonly available plug-in adapters, an interactive debugger in Forth programming language, boot configuration maintenance to enable plug and play, a client interface for the system operating system during boot, a graphical unit interface toolkit for changing boot screen icons and functions, and a Flash update utility to flash program the boot ROM and MacROM.




- Several operating systems are or will be supported with Long Trail. The Long Trail platform is being used in the development of CHRP MacOS 1.0. Long Trail is also a regression platform used by Apple Computer for the development of Tempo, or MacOS 8.0.
- An effort is underway to port BeOS to the Long Trail design. BeOS is a high end graphics, multi-processor operating system.
- It is intended for Long Trail to also run with the future operating system for network computers, JavaOS. Porting JavaOS to Long Trail is underway.
- Long Trail is currently running AIX 4.2x. AIX is a robust high-availability Unix-type server OS.

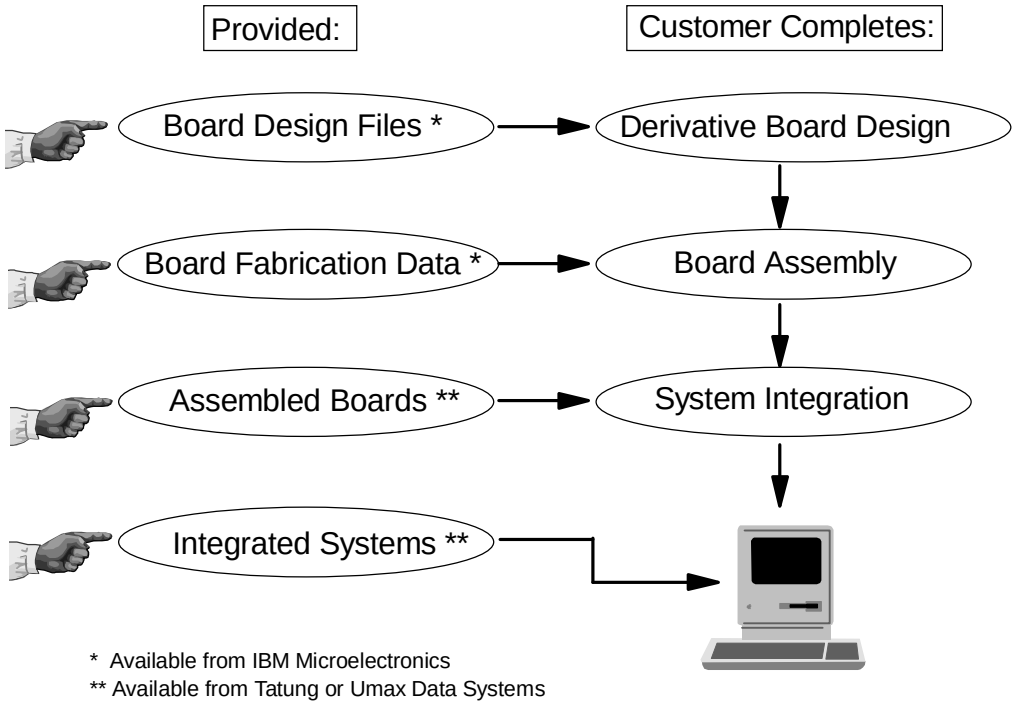
# Long Trail Product Opportunities

## Point-Of-Entry Options

## Derivative Design Examples

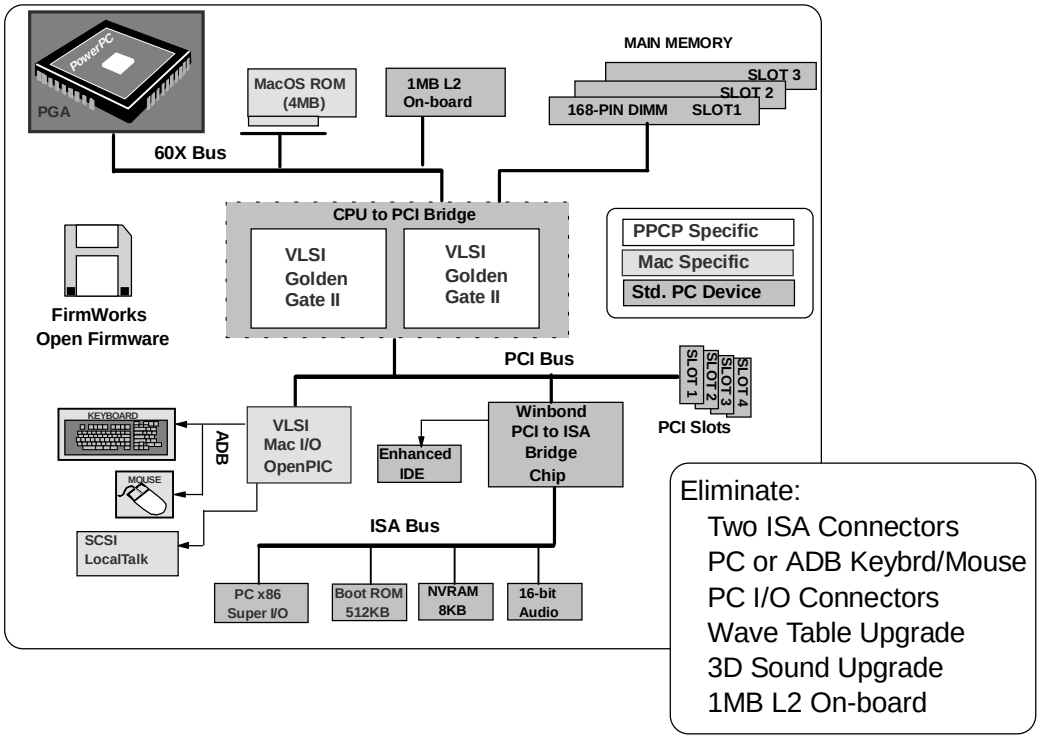
- We can now discuss Long Trail product opportunities.

# Long Trail - Point of Entry Options



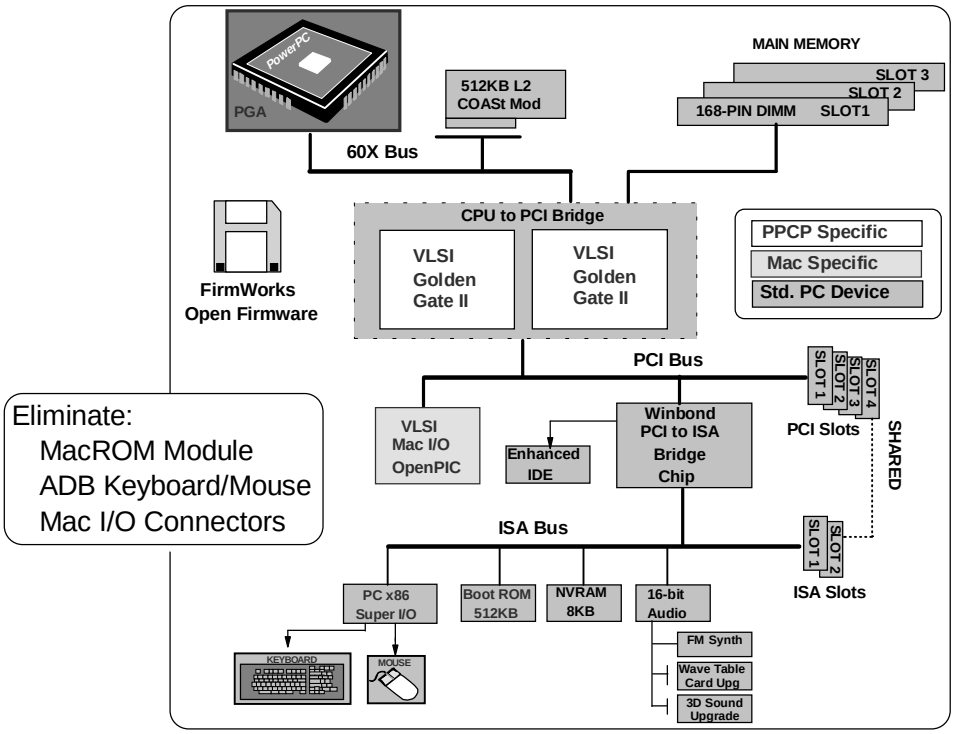

- There are many point of entry options for Long Trail customers. They range from initial board design files to completly integrated systems. The IBM Microelectronics World Wide Design Center in Austin, Texas can provide board design and assembly files along with support for derivative design and bringup. Assembled Long Trail and derivative design boards, and integrated systems are planned to be available from Tatung or Umax Data Systems.

# Derivative Design - MacOS Only




- The Long Trail reference design can easily be altered for a specific implementation. For example, if the ultimate product in a MacOS only system, several components can be deleted, including:  the two ISA connectors, the PC or ADB keyboard and mouse connectors, the PC I/O serial and parallel port connectors, and the Wave Table and 3D sound upgrade connectors.  After gaining the extra real estate from removing unneeded features, further cost reduction can be accomplished also by putting the level two cache on-board, for example.

# Derivative Design - Server




- Another common Long Trail derivative design might be for the server industry. In this case, much of the Macintosh OS specific components can be eliminated, such as: the MacROM module, the ADB keyboard and mouse connectors, and the Mac I/O connectors.

# IBM Design Support

**"Complete platform solution" -- offered by IBM**

- Includes:
  - Technical Specification
  - Schematics and BOM
  - Placement and Mechanical Drawings
  - Physical Design Guide and Selected Component Data
  - Industry Firmware Solutions
  - MacOS port
- On-line technical information:
  - Introductory: http://www.chips.ibm.com/products/ppc
  - Design: ftp://ftp.austin.ibm.com path:/pub/PPC_support/reference_designs/longtrail

- Extensive technical support is offered by IBM Microelectronics World Wide Design Center to customers either directly cloning the Long Trail design or implementing a derivative design. Specifications, schematics, software, and all design files, and are supplied upon request. VLSI Technology, Inc. and FirmWorks, Inc. are also available to provide support to developers of Long Trial derivative designs.
- The near term and most probable implementation of Long Trail will be in support of a PPCP compliant version of MacOS, scheduled for release by Apple in 3Q97. The Long Trail reference design and engineering team will enable third party OEM suppliers to offer a low cost, open-architecture MacOS based system.