

2.4.2 APX-IGGS System Interface (Figures 2-73 through 2-75)

The system interface circuitry decodes all I/O requests sent to the APX-IGGS circuit board, and selects the appropriate devices for access. This circuit also provides support for DMA mode transfers to the 7220 GDC. ICs 2A and 3A provide gating for the I/O read and write signals ($\overline{\text{IOR}}$ and $\overline{\text{IOWR}}$), which are applied to pins 9 and 10, respectively, on the 7220 GDC. The gated read signal on pin 6 of 2A is also used to switch the direction of the LS245 (1B) bus transceiver. The output of IC 2A pin 6 provides the gating signal; this output is high whenever a read or write to port 038H or 039H is issued by the active CPU, or a DMA transfer acknowledge occurs.

ICs 2A, 3A, and 4A are used to implement the I/O address decoder for the APX-IGGS board, which is mapped to the addresses 02AH, 038H, 039H and 03AH. Port 02AH is used to decode the type of display board installed in the system. When port 02AH is accessed by a read or write command, the 2Y0 output on pin 9 of 4A pulls bit 0 on the data bus to ground, signifying that an APX-IGGS circuit board is installed.

The 1Y0 and 1Y1 open-collector outputs of 4A on pins 6 and 7 are tied together and used to enable the $\overline{\text{IOR}}$ and $\overline{\text{IOWR}}$ signals when the active CPU accesses port 038H or 039H. The 1Y2 output on pin 5 is active low when port 03AH is accessed, and is used to write bit 7 and the lower four bits of the data bus into the GAAPGD gate array.

ICs 2A, 6A, and 7A are used to implement DMA transfer handshaking logic. The DMA acknowledge input ($\overline{\text{DACK2}}$) is normally high and applied to pin 1 of IC 6A. This enables the $\overline{\text{DREQ2}}$ output on pin 3 to go low whenever the 7220 requests DMA service. When the request is acknowledged, pin 1 goes low and the output on pin 3 returns to high.

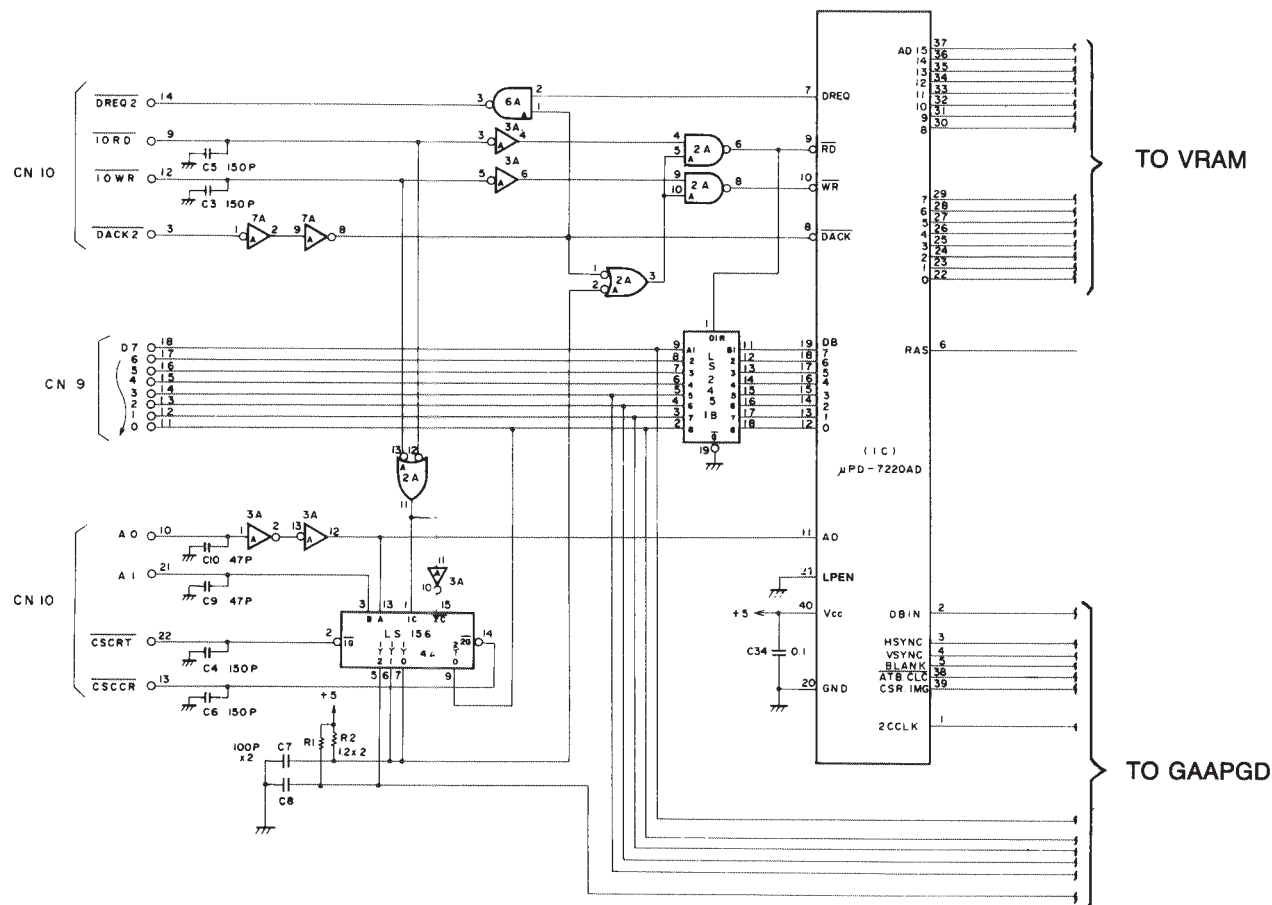


FIGURE 2-73. APX-IGGS SYSTEM INTERFACE CIRCUIT

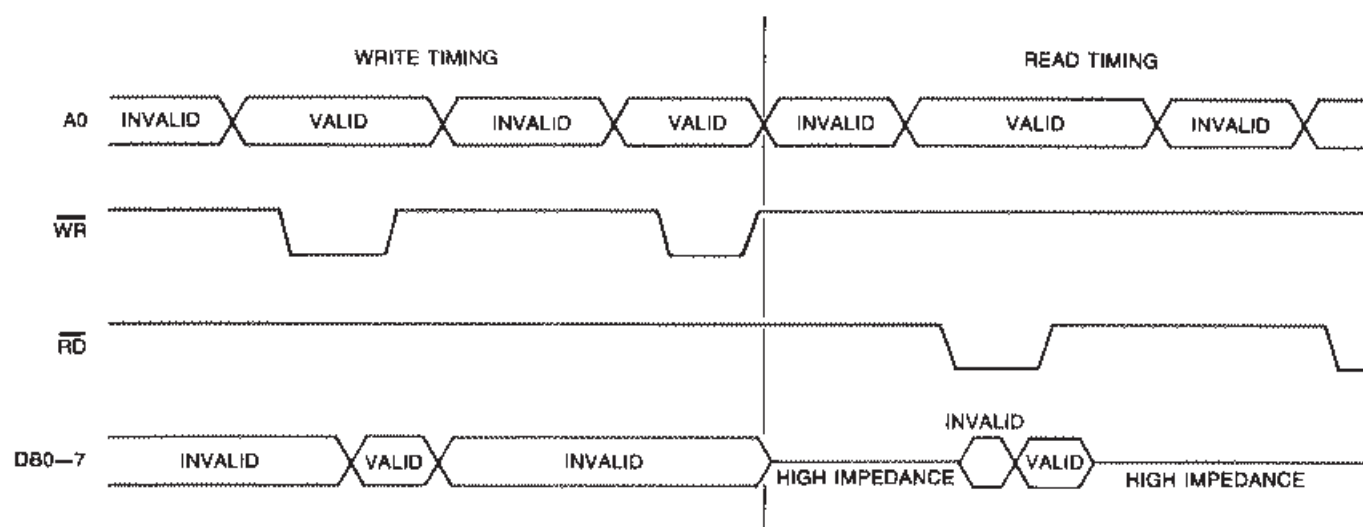


FIGURE 2-74. SYSTEM I/O READ/WRITE TIMING

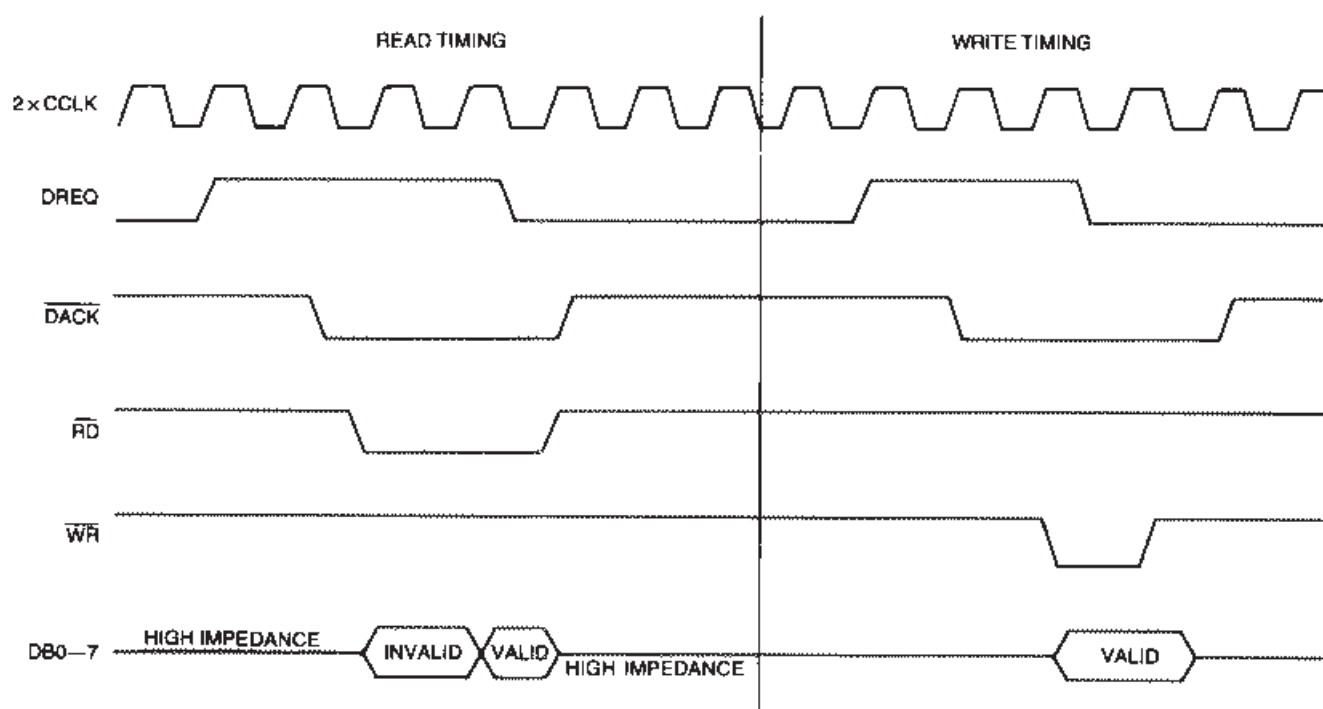


FIGURE 2-75. SYSTEM DMA READ/WRITE TIMING

2.4.3 7220 Graphic Display Controller (Figures 2-76 through 2-79)

The 7220 GDC is an advanced, LSI peripheral chip, which generates a high-resolution raster display and manages the display memory. The GDC is also responsible for carrying out high-level commands issued by the active CPU on the APX-ISYM board for graphics and display functions such as zoom, scrolling, and figure drawing.

The 2CCLK input on pin 1 of the GDC is a 4 MHz signal output from pin 9 of the GAAPGD. The signal originates at oscillator CR1 (16 MHz).

In the QX-16, the 7220 is an I/O device mapped to two different addresses. The \overline{RD} and \overline{WR} signals are brought low by the system interface whenever the active CPU accesses port 038H or 039H. The 7220 does not have a chip select input; access to the internal registers is determined by the status of address bit A0 when RD and WR lines are made active low. (Refer to Table 2-38 for internal register selection.)

Lines AD0-15 on the 7220 are multiplexed address and data lines used for display generation and VRAM updating. The \overline{RAS} output on pin 6 of the 7220 is used to latch the display address into the external address latches and to generate proper timing of the memory signals by the GAAPGD. When the DBIN output on pin 2 of the GDC is low, the GAAPGD and the bus transceivers are signaled that the 7220 is requesting data at the specified location for a display memory update cycle.

The timing signals for the raster display are output from the 7220 to the GAAPGD for output to the CRT. VSYNC is the vertical synchronization signal used to reset the scan of the CRT to the upper left corner. HSYNC is the horizontal synchronization signal used to reset the scan of the CRT to the left side to prepare for the next scan.

Display attribute control is performed by the GAAPGD, and the GDC outputs the ATB.CLC signal which supplies the timing for the blinking attribute.

Organization of the display memory for graphic, text, or mixed mode is controlled by the GAAPGD based on the BLANK and CSR IMG signals output by the GDC. Character mode is selected when CSR IMG is low during an active blanking cycle; graphic mode is selected when CSR IMG is high during blanking.

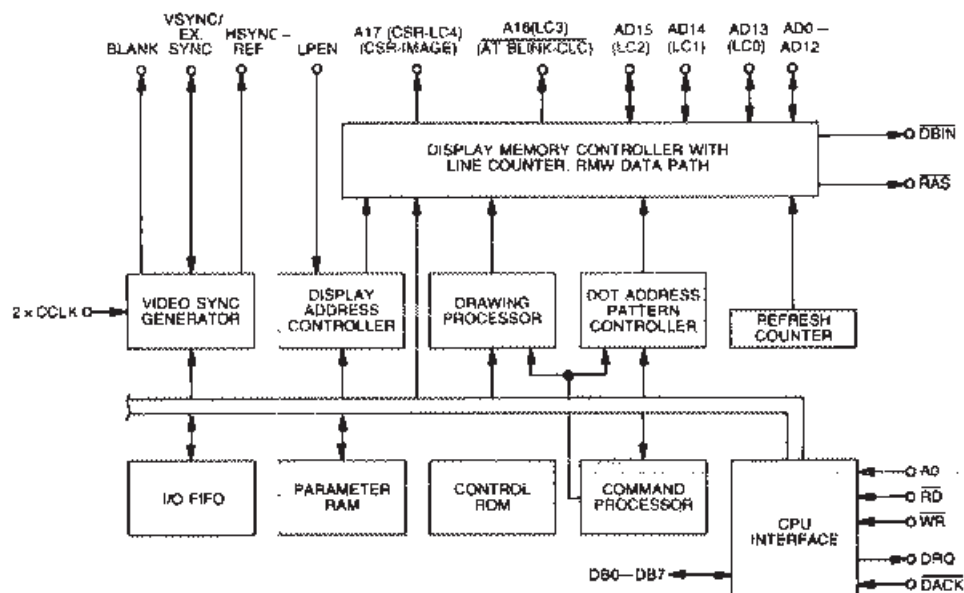


FIGURE 2-76. 7220 GDC BLOCK DIAGRAM

TABLE 2-38. 7220 REGISTER SELECTION

A0	RD	WR	MODE
0	0	1	Reads status flag
1	0	1	Reads data (from GDC)
0	1	0	Writes parameter
1	1	0	Writes command

TABLE 2-39. 7220 PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION																				
22-34	AD0-AD12	IN/OUT	Bidirectional address bus lines																				
35-37	AD13 (LC0) AD14 (LC1) AD15 (LC2) AD16 (LC3)	IN/OUT	During graphic and character-graphic mixed mode: address bus lines. During character mode: line counter.																				
12-19	DB0-DB7	IN/OUT	Bidirectional data bus																				
6	RAS	OUT	Memory control signal output from GDC to VRAM, also used as the timing signal to latch address. CAS is generated from this.																				
38	AT BLINK-CLC	OUT	During blanking time (BLANK signal output): Clears the line counter. During tracing time (video signal output): Outputs attribute blinking timing signals.																				
39	CSR-IMAGE	OUT	During blanking time (BLANK signal output): Outputs cursor mark. During tracing time (video signal output): Outputs character/graphic area switching timing signal.																				
11	A0	IN	Connected to an address line of the CPU and used to designate internal registers. <table data-bbox="722 1102 1193 1249"> <tr> <th>A0</th><th>RD</th><th>WR</th><th>FUNCTION</th></tr> <tr> <td>0</td><td>0</td><td>1</td><td>Read status flag</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>Read data</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>Write parameter</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>Write command</td></tr> </table>	A0	RD	WR	FUNCTION	0	0	1	Read status flag	1	0	1	Read data	0	1	0	Write parameter	1	1	0	Write command
A0	RD	WR	FUNCTION																				
0	0	1	Read status flag																				
1	0	1	Read data																				
0	1	0	Write parameter																				
1	1	0	Write command																				
8	DACK	IN	Supplied from the DMA controller to enable the GDC to distinguish between read and write performed by DMA.																				
7	DREQ	OUT	DMA request																				
2	DBIN	OUT	Memory control signal output from the GDC to VRAM (timing signal used to put VRAM output to the data bus).																				
4	V.SYNC	OUT	Vertical sync signal																				
3	H.SYNC	OUT	Horizontal sync signal																				
5	BLANK	OUT	Blanking signal output during horizontal retrace time, vertical retrace time, time between execution of SYNC and START commands, and draw execution time																				
1	2XCCLK	IN	Supplied from an external dot clock generator. The clock frequency is determined by the relationship between the horizontal resolution in dots and the horizontal scanning time (4MHz).																				
9	RD	IN	Used in combination with A0 to read status and data from 7220.																				
10	WR	IN	Used in combination with A0 to write commands and parameters to the 7220																				

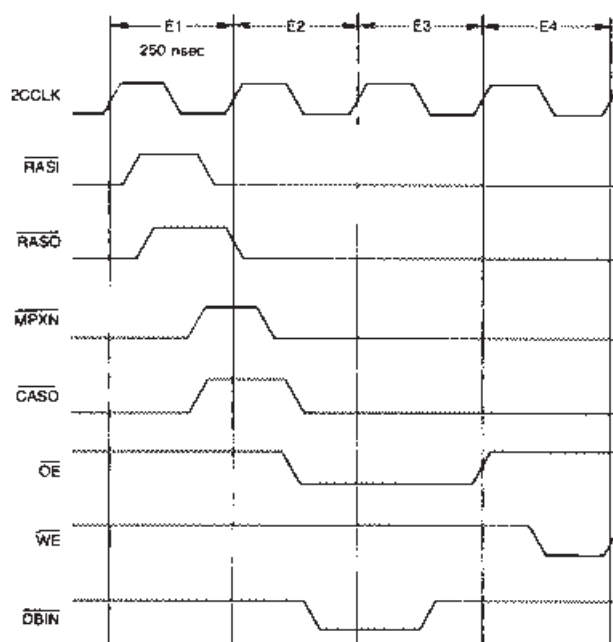


FIGURE 2-77. VRAM TIMING DIAGRAM

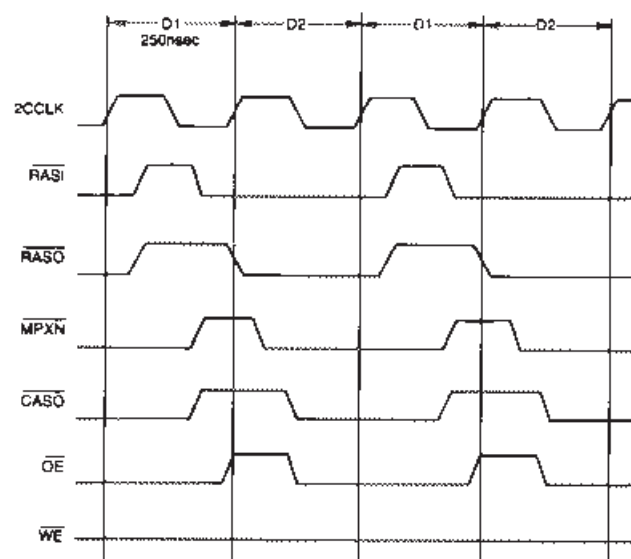


FIGURE 2-78. DISPLAY MODE TIMING DIAGRAM

2.4.4 GAAPGD LSI Gate Array (Figure 2-79)

The GAAPGD LSI gate array receives input signals from the 7220 and the active CPU and converts these to VRAM timing control signals for the RAM and APX-IGGS bus control devices. Control of the VRAM on the APX-IGGS board is dependent upon the hardware zoom register, accessed as port 03AH. When the zoom register is accessed, the lower four bits (ZOM 0-3) and bit 7 (STOP) of the data bus are written into the GAAPGD gate array. Bits 0-3 are used for controlling the row and column counters, and bit 7 is used to disable the video output signals from the GAAPGD.

The $\overline{\text{RAS}}$ (pin 2) and $\overline{\text{DBIN}}$ (pin 3) inputs are used to generate the memory timing signal outputs from the GAAPGD. $\overline{\text{MPXN}}$ (pin 47) is used as the enable signal for the column address latch (3B). $\overline{\text{MPXP}}$ is the enable signal for the row address latch (2B). These signals are used in conjunction with the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals to strobe in the row and column addresses for the VRAM.

Write enable ($\overline{\text{WE}}$) is used to write the 7220 bus data into the VRAMs. The output enable ($\overline{\text{OE}}$) signal is used to read the contents of the VRAMs onto the bus during display or update cycles. The DLAT signal (pin 38) is used to latch the data from the VRAMs into the VRAM data latches (ICs 8C and 9C).

The LGTI, RVS, SCRT and BLINK inputs (pins 39-42) are the attribute inputs to the GAAPGD from the VRAM data latch (9C). Outputs LC0-3 (pins 33-35 and 37) are supplied from the line counter circuitry to the character generator (6D) when the display is in character mode.

The IMG output on pin 22 is active low during the character display mode to enable the outputs of the character generator; this output is high during graphic mode. The HB and LB signals (pins 22-23) are used to successively load the high and low bytes of the VRAM data latches into the GAAPGD during graphics mode operation. The video dot patterns loaded into the GAAPGD by the IMG, HB and LB signals are shifted out of the $\overline{\text{VIDE}}$ output on pin 21. If the display is in graphics mode, the highlight signal $\overline{\text{LGTO}}$ (pin 20) is low; $\overline{\text{LGTO}}$ is active high when the display is in character mode and the high intensity or bright attribute is set. $\overline{\text{VSOT}}$ and $\overline{\text{HSOT}}$ are the vertical and horizontal synchronization signals, respectively. The $\overline{\text{VIDE}}$, $\overline{\text{LGTO}}$, $\overline{\text{VSOT}}$ and $\overline{\text{HSOT}}$ signals are all disabled when the STOP (bit 7) input is high during a write to port 03AH.

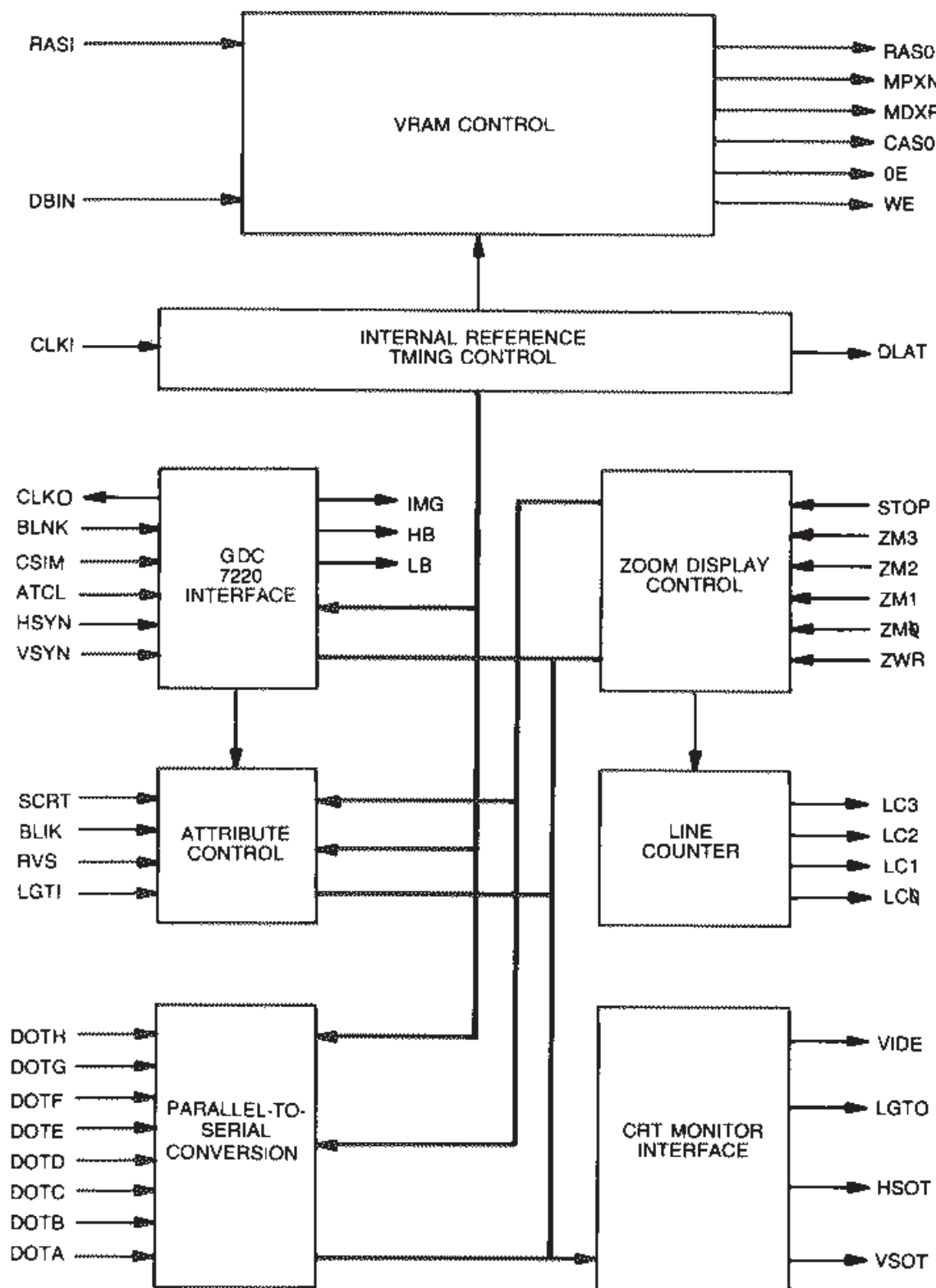


FIGURE 2-79. GAAPGD LSI BLOCK DIAGRAM

TABLE 2-40. GAAPGD PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	CLKI	IN	Clock input from CR1.
2	RASI	IN	RAS memory timing signal from 7220
3	DBIN	IN	Used to read data from VRAM into 7220.
9	CLKO	OUT	CLKI input frequency is divided by four and applied to 7220 2xCCLK input.
48	RASO	OUT	RAS timing signal for VRAM devices. Based on RASI input.
47	MPXN	OUT	Active low signal to enable column address latch onto VRAM address bus.
46	MPXP	OUT	Active low signal to enable row address latch onto VRAM address bus.
45	CASO	OUT	CAS timing signal for VRAM devices.
44	WE	OUT	Write enable signal for VRAMs.
43	OE	OUT	Active low to read contents of VRAM.
38	DLAT	OUT	Latches VRAM data into 8C and 9C.
7	HSYN	IN	Horizontal sync signal from 7220
8	VSYN	IN	Vertical sync signal from 7220.
4	BLANK	IN	Blanking signal from 7220
5	ATCL	IN	Attribute clock signal from 7220.
6	CSIM	IN	Cursor/display mode signal from 7220
16-19	ZOM0-3	IN	Zoom port inputs from data bus.
15	STOP	IN	Stop signal; latched-in with zoom value.
14	ZWR	IN	Zoom port clock input; active low.
21	VIDE	OUT	Video dot signal to CRT.
20	LGTO	OUT	Intensity signal for CRT.
10	HSOT	OUT	Horizontal sync output to CRT.
11	VSOT	OUT	Vertical sync output to CRT.
33-35,37	LC0-3	OUT	Line counter outputs for 2764 character generator.
22	IMG	OUT	Enables character generator outputs in alphanumeric mode.
24	LB	OUT	Enables low byte of graphics word into GAAPGD.
25	HB	OUT	Enables high byte of graphics word into GAAPGD.
42	LGTI	IN	Highlight attribute signal.
41	RVS	IN	Reverse attribute signal.
40	SCRT	IN	Secret attribute signal.
39	BLINK	IN	Blinking attribute signal.

2.4.5 VRAM Memory Circuit (Figure 2-80)

The VRAM circuit is used to store the contents of the display image in graphics mode and the character code and attribute data in alphanumeric mode. The circuitry consists of the memory devices, address latches and the bus transceivers.

The row and column address latches hold the display memory address during VRAM memory cycles. The address is latched in by the $\overline{\text{RAS}}$ signal (1C pin 6) and the outputs of the latches are selectively enabled to coincide with the $\overline{\text{RASO}}$ and $\overline{\text{CASO}}$ signals from the GAAPGD.

The bus transceivers (ICs 4B and 5B) are used to control the direction of information between the GDC and the VRAMs. These devices are enabled by the $\overline{\text{RASO}}$ signal (IC 3C pin 48) while the memory address is being loaded into the RAMs by the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ control lines. The direction is selected by the DBIN signal from the GDC, which is active low when it is reading from display memory.

The memory devices are very similar to those used on the APX-LSYM circuit board, with the exception of the output enable ($\overline{\text{OE}}$) pin. This active low signal is required for controlling the common data input/output lines, and is generated by the GAAPGD to enable the RAMs when the GDC needs information, or when data is to be output to the display.

Table 2-41 describes the function of the memory address bits for character and graphic modes.

TABLE 2-41. APX-IGGS VRAM CHIP FUNCTIONS

MODE	IC6B	IC7B	IC8B	IC9B
CHARACTER	ASCII VALUE		BRIGHT REVERSE	FLASHING SECRET
GRAPHIC	LSB \longleftarrow GRAPHICS WORD \longrightarrow MSB			

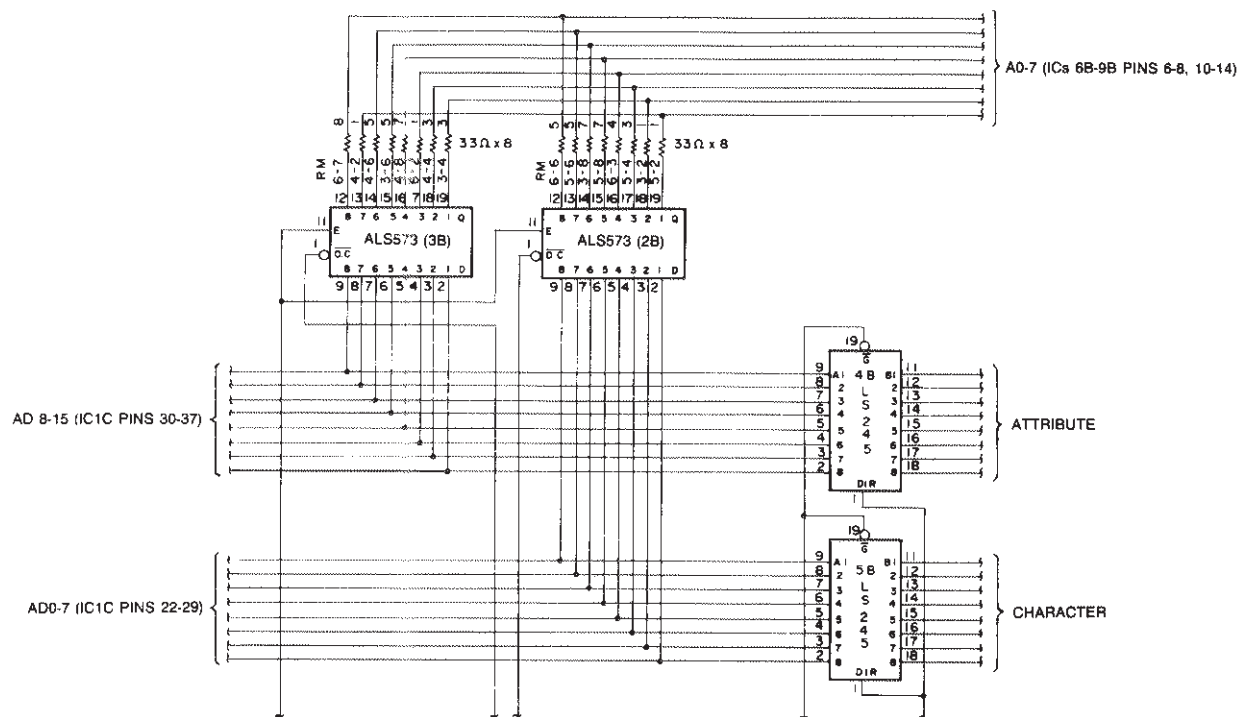


FIGURE 2-80. APX-IGGS VRAM CIRCUIT

2.4.6 Character Generator Circuit (Figure 2-81)

The character generator circuit provides the switching circuitry to output the VRAM information to the GAAPGD gate array as graphic or character data.

The two latches (IC 8C and 9C) store the VRAM data when the DLAT signal (3C pin 38) goes to high. The display mode programmed into the 7220 controls how the data stored in the latches is interpreted. The BLANK and CSR.IMG signals, output by the GDC control circuit, indicate which mode is in effect.

When character mode is selected, the content of latch 8C is interpreted as ASCII character code, and its value is supplied to the character generator address lines A4-A11. Four bits of latch 9C are used as the attribute data for the selected character. Line counter outputs from the GAAPGD are applied to the character generator address bits A0-A3. The GAAPGD chip brings the IMG output (pin 22) low to enable the character generator outputs to be read into the DOT A-H inputs (pins 25-32). Eighty consecutive addresses are repeated 16 times and the line counter value is incremented each time to form one alphanumeric display row. At the end of this process the display row counter is incremented and the process repeats itself for the next alphanumeric display line. This process occurs 24 or 25 times, depending on the display format (80 × 24 or 80 × 25).

When graphic mode is selected, the data in latch 8C is read into the GAAPGD when the LB output (pin 24) goes low. The data in latch 9C is read into the GAAPGD when the HB output (pin 23) goes low. This process is repeated for 40 consecutive addresses to create one scan line. At this point the display row counter is incremented and the process repeats for the next scan line. In graphic mode this process repeats itself 400 times for each display frame.

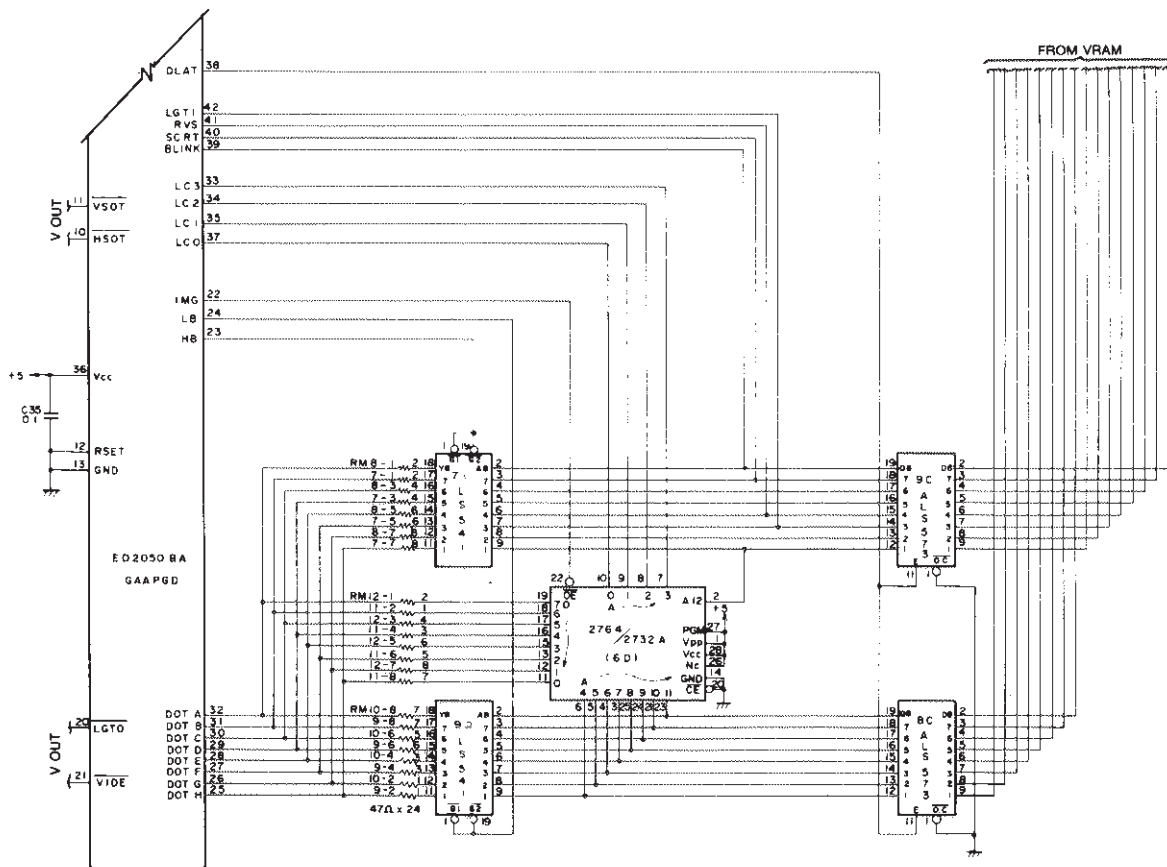


FIGURE 2-81. APX-IGGS CHARACTER GENERATOR CIRCUIT

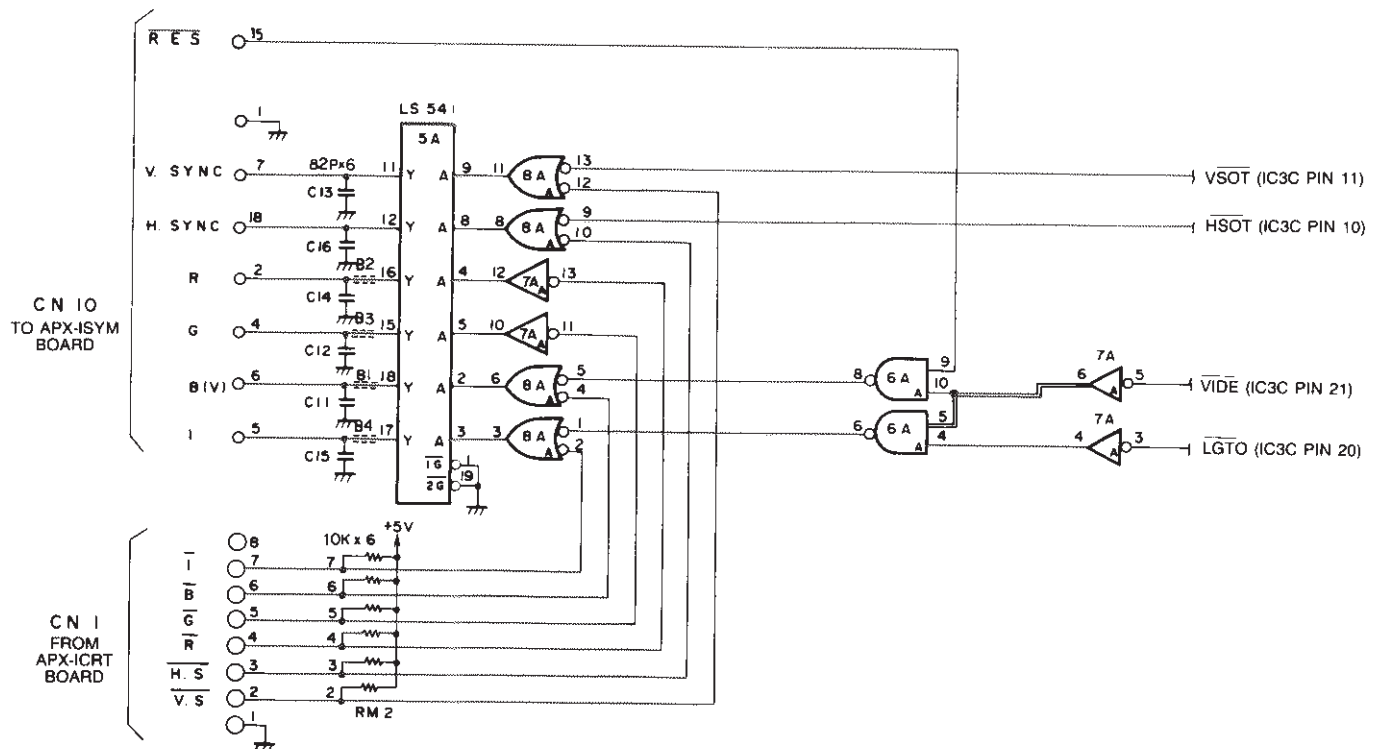
2.4.7 APX-IGGS Output Circuit (Figure 2-82)

The APX-IGGS output circuit, composed of ICs 5A, 6A, 7A, and 8A, combines its outputs with those of the APX-ICRT board. The $\overline{\text{VIDE}}$, $\overline{\text{LGTO}}$, $\overline{\text{VSOT}}$, and $\overline{\text{HSOT}}$ outputs from the GAAPGD are all set high when the STOP input (bit 7) is high during a write to port 03AH. (Refer to Section 2.5.4.) This allows the APX-ICRT outputs, listed in Table 2-42, to drive the LS541 buffer. The APX-ICRT outputs are disabled when bit 7 is low during a write to port 03CFH. For a more detailed description of this port, refer to Section 2.5 and Chapter 6.

TABLE 2-42. APX-IGGS VIDEO INPUT SIGNALS*

CN1 PIN	SIGNAL NAME	FUNCTION
1	GND	Signal ground
2	$\overline{\text{V.S.}}$	Vertical sync
3	$\overline{\text{H.S.}}$	Horizontal sync
4	$\overline{\text{B}}$	Blue video signal
5	$\overline{\text{G}}$	Green video signal
6	$\overline{\text{R}}$	Red video signal
7	$\overline{\text{I}}$	Intensity signal
8	N/C	No connection

*All inputs to the APX-IGGS are from the APX-ICRT board.

**FIGURE 2-82. APX-IGGS VIDEO OUTPUT CIRCUIT**